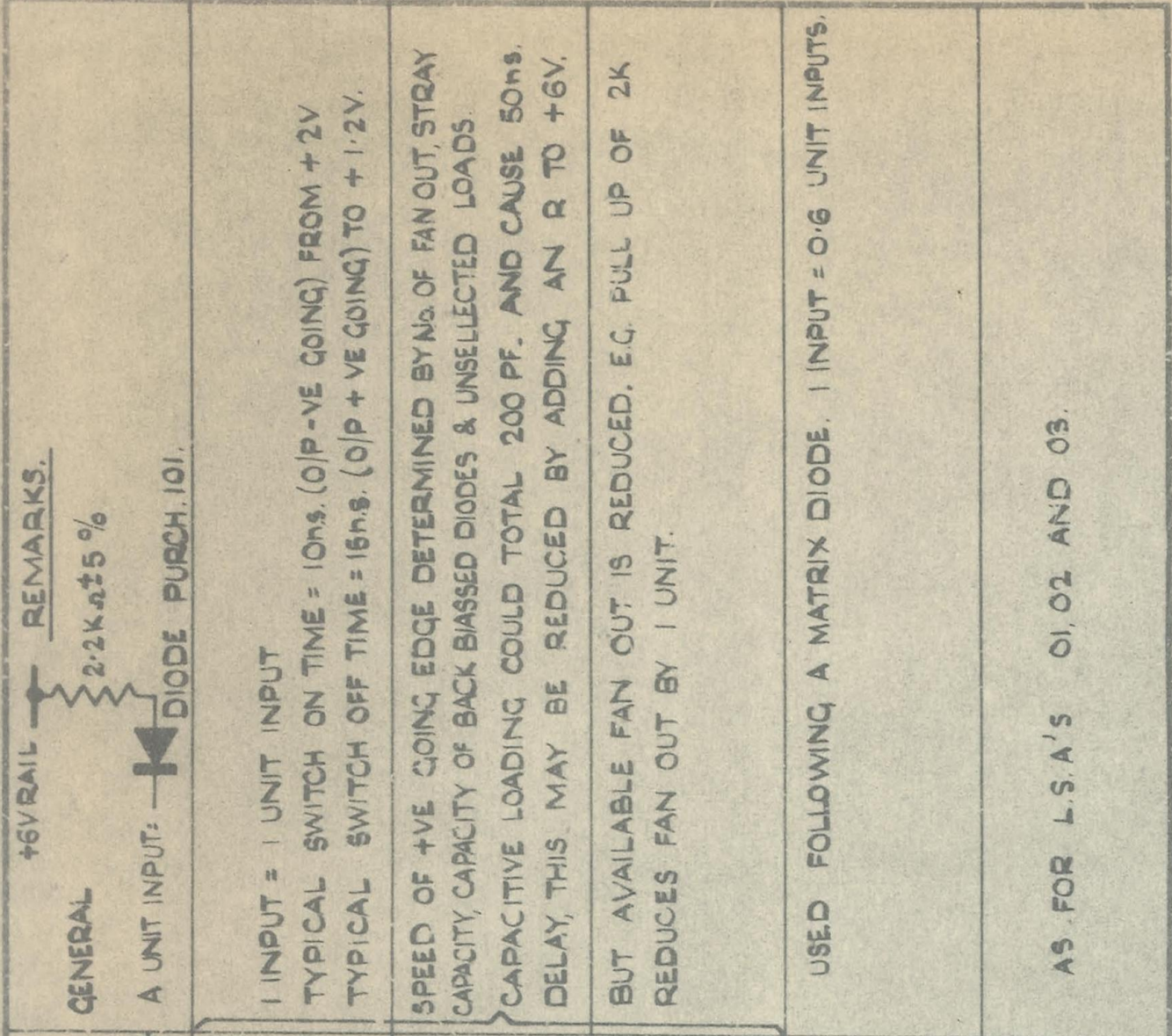


SHT Nº	ISSUE							SHT Nº	ISSUE						
	1	2	3	4	5	6	7		1	2	3	4	5	6	7
1	1	2	3	3				42							
2	1	1	1	1				43							
3	1	1	1	1				44							
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ISSUE	1	2	3	4										
MOD Nº	1374	1505	1588	1796										
DATE	26-4-66	26-4-66	26-8-66	28-11-66										
DRAWN C. CLARKE	DATE 26-4-66			APPVD. <i>R. Homburg</i>			SHEET 1 OF 29							
TITLE 920 B L.S.A. ELEMENT. LOGIC SYMBOLS & CIRCUIT DIAGRAMS.										DRG. Nº 322 A 7191				

1



L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	1/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS			REMARKS.
			0 - 80°C	-20 - 80°C	-40 - 80°C	
01 2 INPUT NAND GATES		1.2	11	9	8	1 INPUT = 1 UNIT INPUT TYPICAL SWITCH ON TIME = 10ns. (O/P - VE GOING) FROM +2V TYPICAL SWITCH OFF TIME = 16ns. (O/P + VE GOING) TO +1.2V.
02 3 INPUT NAND GATES		1.2	11	9	8	SPEED OF +VE GOING EDGE DETERMINED BY No. OF FAN OUT, STRAY CAPACITY, CAPACITY OF BACK BIASED DIODES & UNSELECTED LOADS. CAPACITIVE LOADING COULD TOTAL 200 PF. AND CAUSE 50ns. DELAY, THIS MAY BE REDUCED BY ADDING AN R TO +6V.
03 4 1/P NAND GATE PLUS 2 INVERTERS		1.2	11	9	8	BUT AVAILABLE FAN OUT IS REDUCED. E.G. PULL UP OF 2K REDUCES FAN OUT BY 1 UNIT.
04 CONTROL MATRIX WAVEFORM AMPLIFIERS		2.5	3	2	2	USED FOLLOWING A MATRIX DIODE. 1 INPUT = 0.6 UNIT INPUTS.
05		1.2	11	9	8	AS FOR L.S.A.'S 01, 02 AND 03.

DRAWN C.A.C.
 CHECKED CS 456
 APPROVED *ERT*
 DATE 2/5/66

ISSUE No 1
 A.R. No 1374
 DATE 26-4-66
 INITIALS C.A.C.

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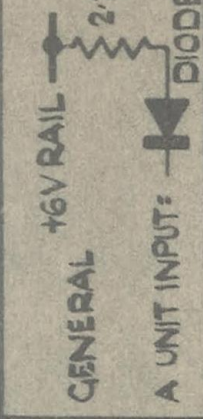
L.S.A. DESIGN NOTES.

INSTRUCTION SHEET

322 A 7191

SHEET No 2

REMARKS



GENERAL
A UNIT INPUT: DIODE PURCH 101.

AS FOR LSA'S 01, 02, AND 03.

$\Delta = 100 \text{ n.s.} \pm 10\%$ 1 INPUT = 3 UNIT INPUTS. USED WITH LSA 08 (2.4V. REF. GEN) LEADS SHOULD BE KEPT SHORT TO AVOID +VE GOING O/P PULSES BEING SHORTENED. SEE NOTES ON C. LOADING IN LSA'S 01, 02 AND 03.

USED AS 2.4 V REFERENCE SUPPLIER TO PULSERS 07, 09, 13 AND 14. A PULSER INPUT FOR THIS LSA = 2.0 UNIT INPUTS.

1 INPUT = 3 UNIT INPUTS. $\Delta = 470 \text{ n.s.} \pm 10\%$ USED WITH LSA 08.

1 INPUT = 1 UNIT INPUT. USED PRECEDING LSA 12 OR LSA 17.

L.S.A. No. AND NAME.	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS.			REMARKS
			-20-80°C	-20-80°C	-40-86°C	
06		1.2	11	9	8	
07 PULSE GENERATORS		2.4	17	16	14	
08 VOLTAGE REFERENCE		-	50	50	50	
09 PULSE GENERATOR		2.4	17	16	14	
11 CABLE TRANS-MITTERS.		1.2	6	4	3	

DRAWN C.A.C.
CHECKED CS 456
APPROVED C.A.C.
DATE 10/5/66

ISSUE No. 1
A.R. No. 1374
DATE 26-4-66
INITIALS C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE
L.S.A. DESIGN NOTES.

INSTRUCTION SHEET
322A 7191

SHEET No. 3
OF

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FANOUT LOAD IN UNIT INPUTS			REMARKS
			0-80°C	-20-80°C	-40-80°C	
12 CABLE RECEIVERS		2.0	31	30	26	<p>GENERAL</p> <p>+6V RAIL 2.2kΩ ± 5% A UNIT INPUT - DIODE PURCH 101</p> <p>USED FOLLOWING LSA 11 - FAN OUT CALC. WHEN CONNECTED TO LSA 11.</p>
13 PULSE GENERATORS		2.4	17	16	14	1 INPUT = 9 UNIT INPUTS. Δ = 330 ns. ± 10% USED WITH LSA 08.
14 PULSE GENERATOR		2.4	17	16	14	1 INPUT = 3 UNIT INPUTS. Δ = 660 ns. ± 10% USED WITH LSA 08
15 2 I/P NAND GATE PLUS 2 INVERTING DRIVERS.		1.2	19	16	14	1 INPUT = 2.2 UNIT INPUTS. LARGER FAN OUT THAN LSA 01 ETC. 390Ω PULL UP AT O/P PROVIDES GOOD +VE EDGES. SUITABLE FOR GATEING 100ns. PULSE INTO REGISTERS. AS FOR LSA'S 01, 02 AND 03.
16 F-MINILOG DRIVERS.		1.2	9	8	7	1 INPUT = 2.2 UNIT INPUTS. LARGER FAN OUT THAN LSA 01 ETC. 390Ω PULL UP AT O/P PROVIDES GOOD +VE EDGES. SUITABLE FOR GATEING 100ns. PULSE INTO REGISTERS. 1 INPUT = 1 UNIT INPUT.

DRAWN C.A.C. ISSUE No. 1
 CHECKED CS456 A.R. No. 1374
 APPROVED R.W. DATE 26-4-66
 DATE 10/5/66 INITIALS C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

L.S.A. DESIGN NOTES.

INSTRUCTION SHEET

322A7191

SHEET No 4 OF

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS			REMARKS
			0-80°C	-20-90°C	-40-80°C	
17 PAPER TAPE RECEIVER.		2.0	30	29	25	GENERAL +6V RAIL 2.2k $\pm 5\%$ A UNIT INPUT: DIODE PURCH 101 USED FOLLOWING LSA 11 - FAN OUT CALC. WHEN CONNECTED TO LSA 11.
18 SINGLE I/P NOISE REJECTION INVERTORS		2.0	28	26	23	1 INPUT = 2.2 UNIT INPUTS. USUALLY USED FOLLOWING A KEY SWITCH TO AVOID SWITCH NOISE. $\Delta \pm 1ms.$
19 & 20 DELAY		3.0	20	19	17	1 INPUT = 1 UNIT INPUT. USUALLY USED IN POWER SUPPLY LOGIC. $\Delta \pm 94ms.$
19 & 21 DELAY		3.0	20	19	17	1 INPUT = 1 UNIT INPUT. USUALLY USED IN POWER SUPPLY LOGIC. $\Delta \pm 22ms.$
22 TWO I/P TRANSMITTERS.		0				1 INPUT = 2.2 UNIT INPUTS. USED PRECEDING LSA 23. DATA O/P TO 50 Ω COAX. MAY DRIVE UP TO 2 SELECTED AND 10 UNSELECTED LSA 23'S.

DRAWN C.A.C.
 CHECKED CS456
 APPROVED *[Signature]*
 DATE 10/5/66

ISSUE No. 1
 AS No. 1374
 DATE 26-4-66
 INITIALS C.A.C.

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L.S.A. DESIGN NOTES.

INSTRUCTION SHEET

322A 7191

SHEET No 5 OF

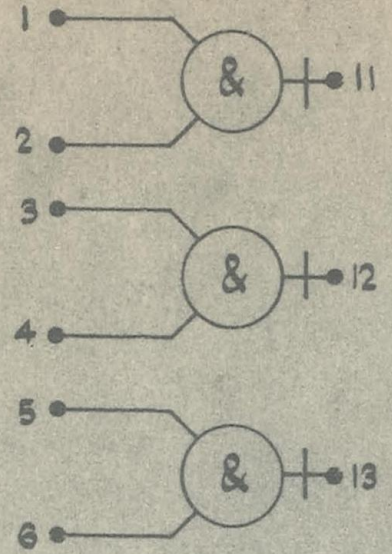
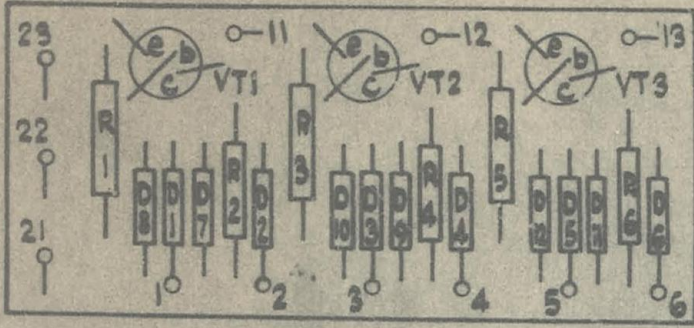
L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS			REMARKS
			0-80°C	-20-80°C	-40-80°C	
23 GATED RECEIVERS		2.0	9	6	4	<p>GENERAL. +6V RAIL 2.2k \pm 5% A UNIT INPUT = DIODE PURCH 101</p> <p>USED WITH L.S.A. 22 25 & 44 DATA INPUT FROM 20' OF 50ms COAX GIVES DELAY FROM I/P LSA 22 TO O/P LSA 23 +VE EDGE IS TYPICALLY 80 n.s. (60 n.s. DUE TO CABLE). -VE EDGE IS TYPICALLY 120 n.s. (60 n.s. DUE TO CABLE).</p>
24-27	USED BY D.R.D.					
28 2 I/P NAND GATES.		1.2	28	26	23	1 INPUT = 2.2 UNIT INPUTS. USED AS A SELECTION DRIVER FOR LSA 29. IN O/P LOADING CALC. A SELECTED LSA 23 = 4.0 UNIT INPUTS AND ANY O/P LOAD ON THE LSA 23 SHOULD BE ADDED TO LSA 28 TOTAL.
43 VOLTAGE RAIL SENSING			1	1	1	
44 2 I/P NAND GATES		1.9 1.2	11	9	8	AS FOR LSA 01, 02 & 03 INPUTS 1, 2 & 5 HAVE A HIGH THRESHOLD FOR USE FOLLOWING AN L.S.A. 23

DRAWN C.A.C. ISSUE No. 1 2 3
 CHECKED CS 156 A.P. No. 1374 1588 1796
 APPR. VED [Signature] DATE 26-4-66 26-8-66 26-11-66
 DATE 16/5/66 INITIALS C.A.C. KG

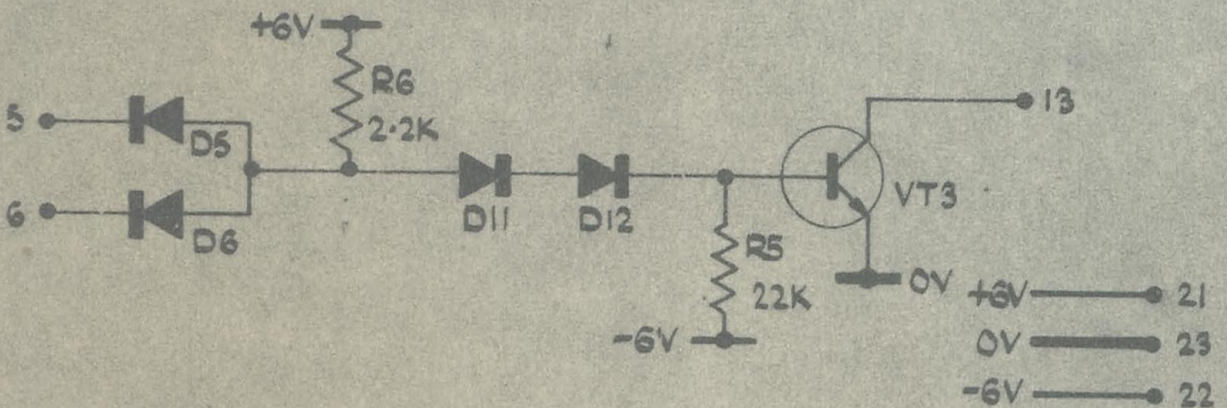
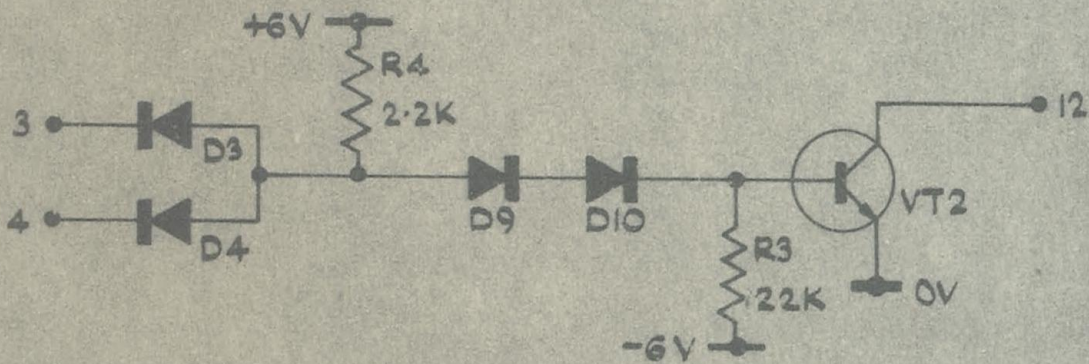
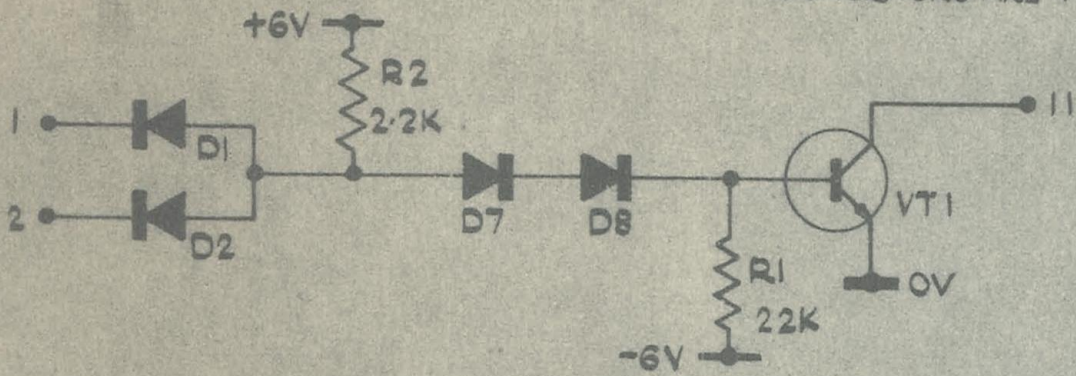
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TITLE
L.S.A. DESIGN NOTES.

INSTRUCTION SHEET
322A 7191
SHEET No 6
OF



DIODES ARE PURCH.101
TRANSISTORS ARE PURCH.100



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APPROVED E.R.H. DATE 26-4-66
DATE 16/5/66 INITIAL C.A.C.

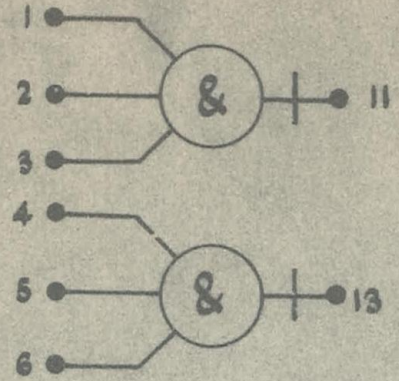
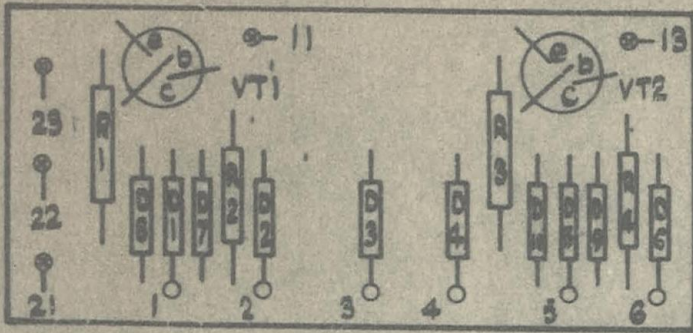
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TITLE
LSA 01
2-INPUT NAND GATE 920B

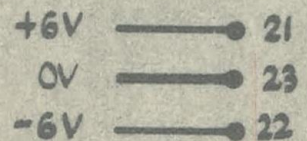
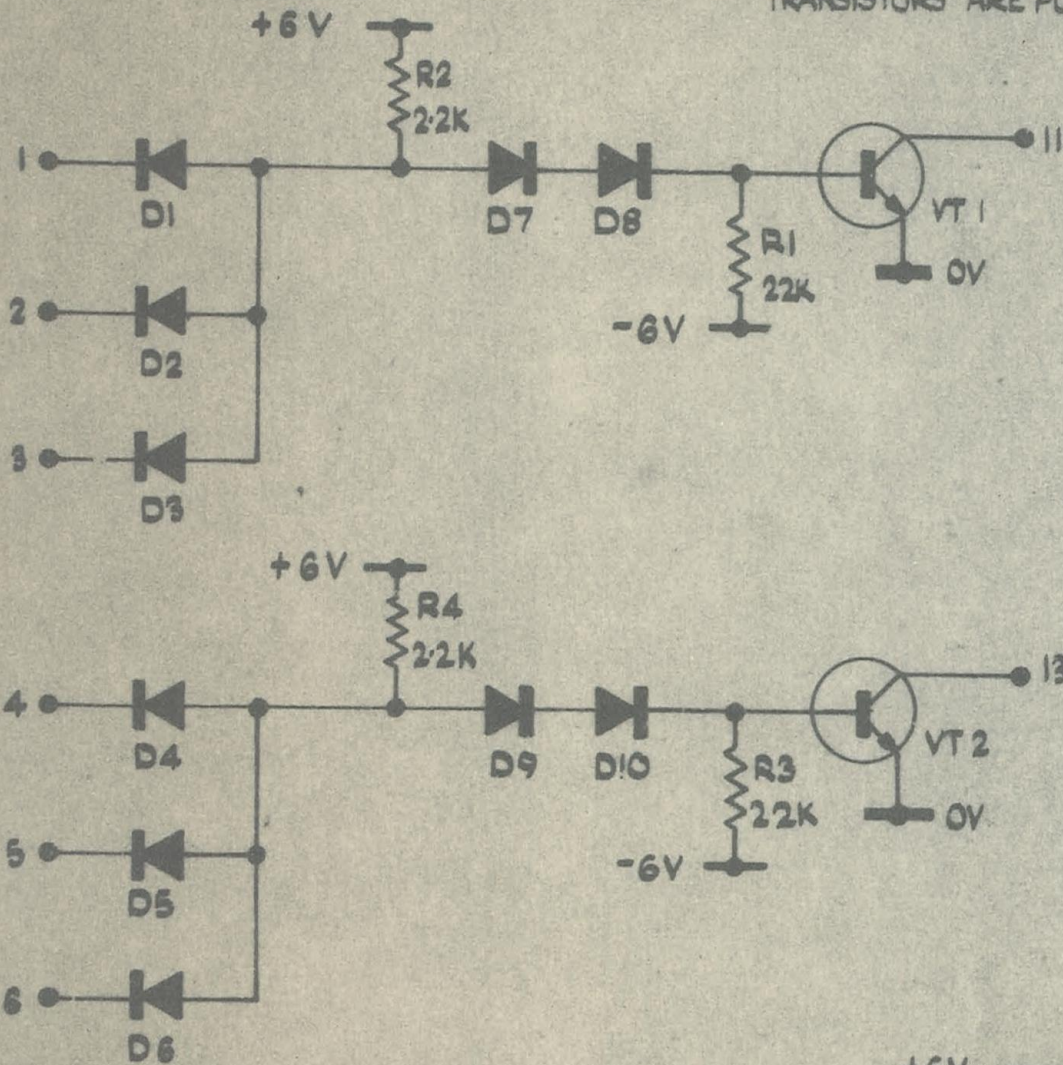
INSTRUCTION SHEET

322A7191

SHEET No 7
OF



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100



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APPR VED	ERM	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

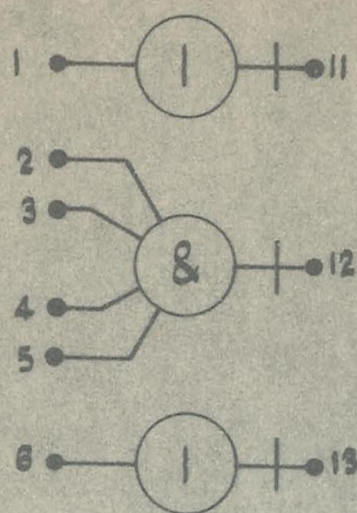
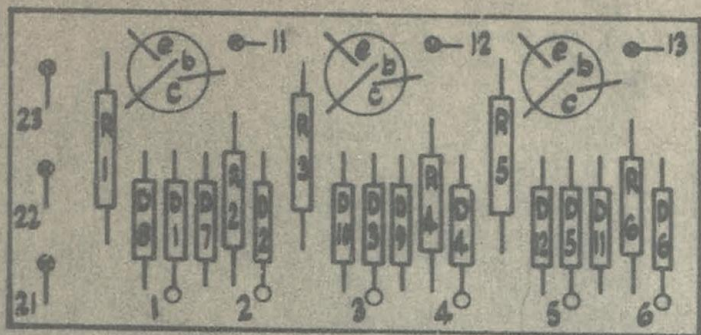
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3 - INPUT NAND GATE 920 B

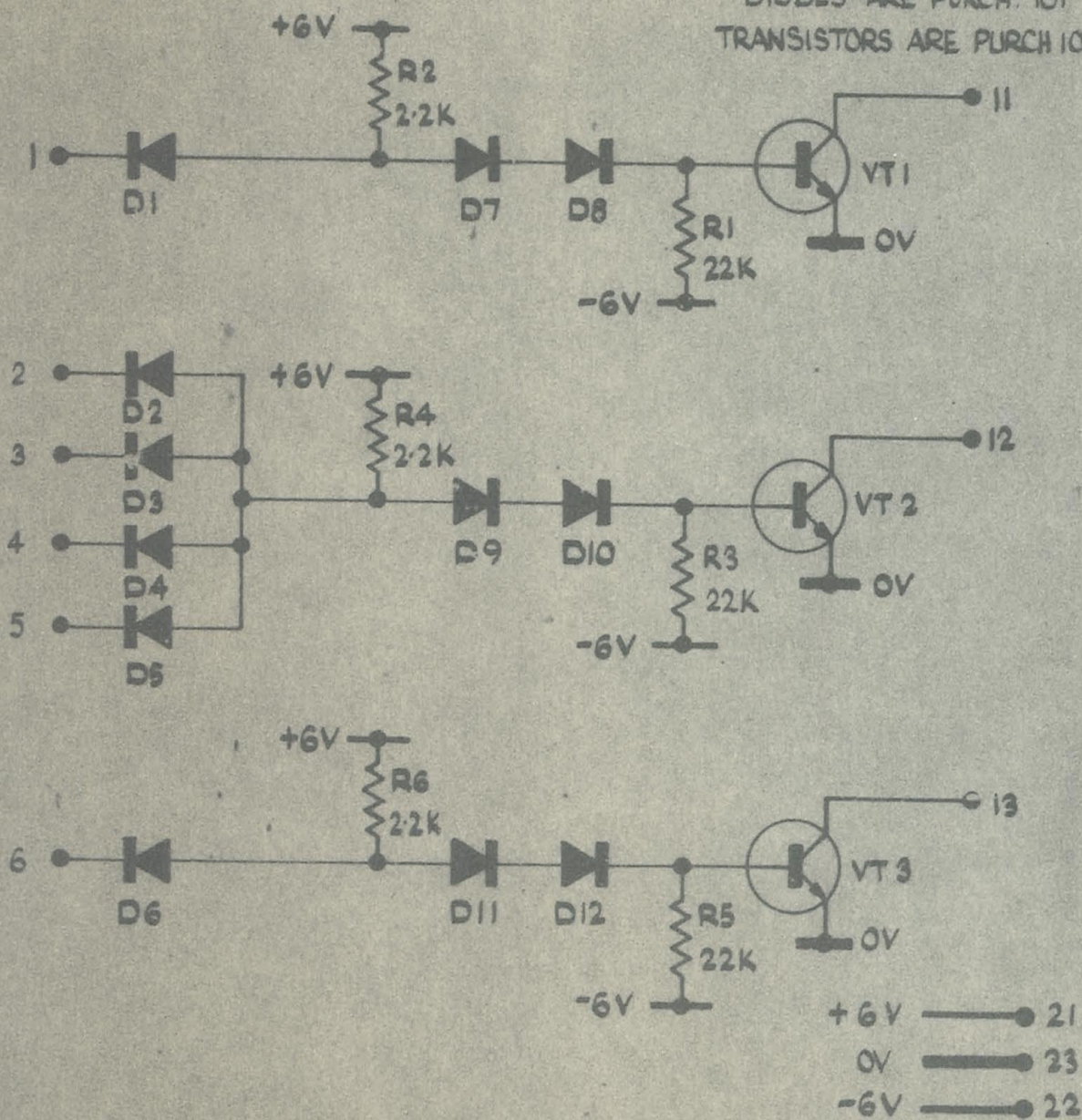
INSTRUCTION SHEET

322 A7191

SHEET No 8
OF



DIODES ARE PURCH. 101
TRANSISTORS ARE PURCH 100



DRAWN	C.A.C.	ISSUE No.	1
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APPROVED	<i>[Signature]</i>	DATE	26-4-66
DATE	6/5/66	INITIALS	C.A.C.

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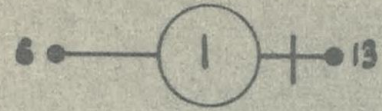
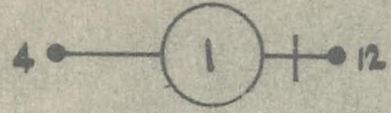
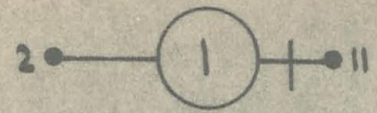
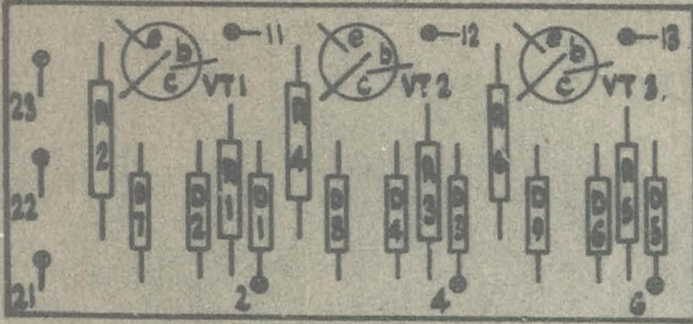
TITLE

L.S.A. 03
4-INPUT NAND GATE + 2 INVERTERS 920B

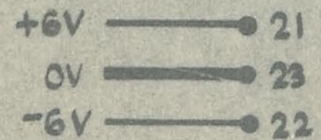
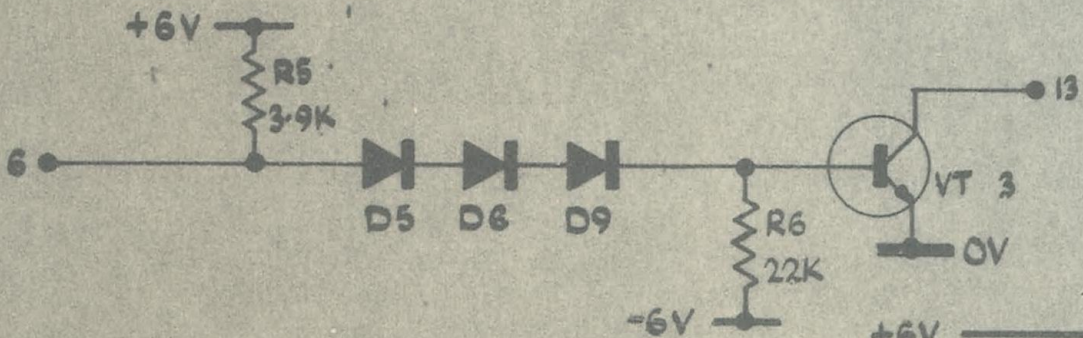
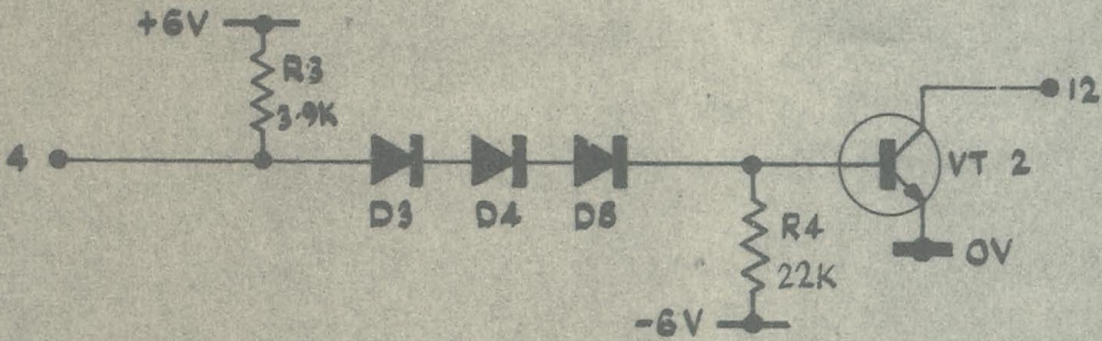
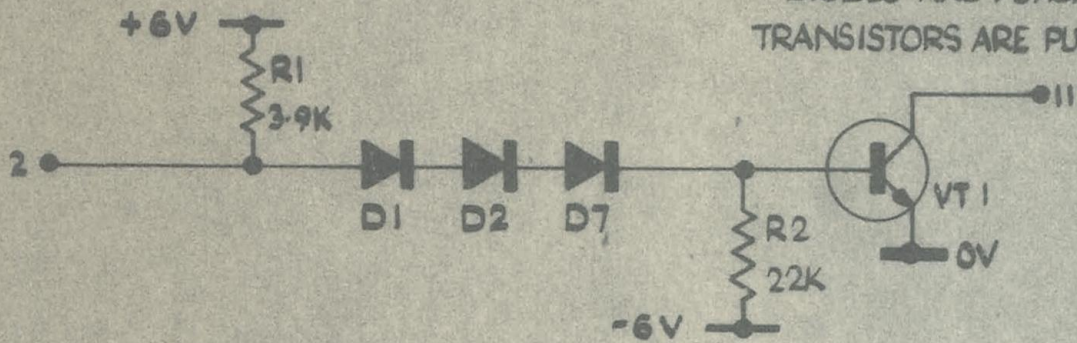
INSTRUCTION SHEET

322A7191

SHEET No 9
OF



DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.



DRAWN	C.A.C.	ISSUE No.	1
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APPROVED	<i>[Signature]</i>	DATE	26-4-66
DATE	10/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

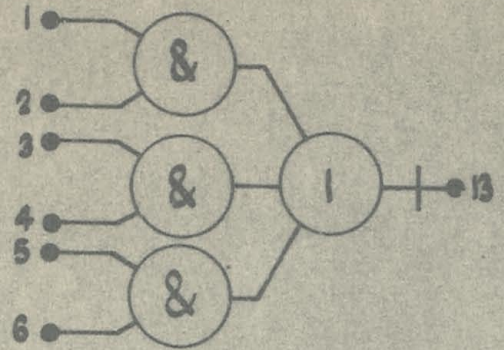
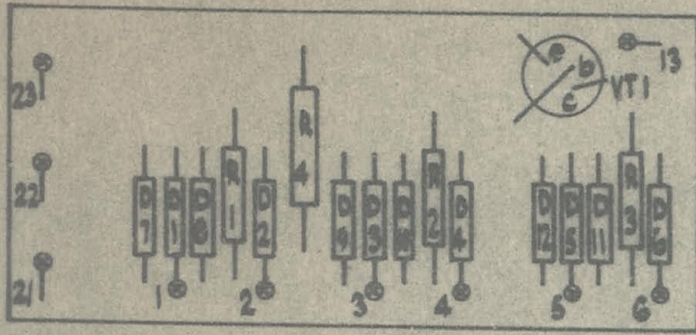
L.S.A. 04

INSTRUCTION SHEET

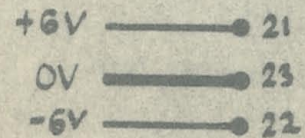
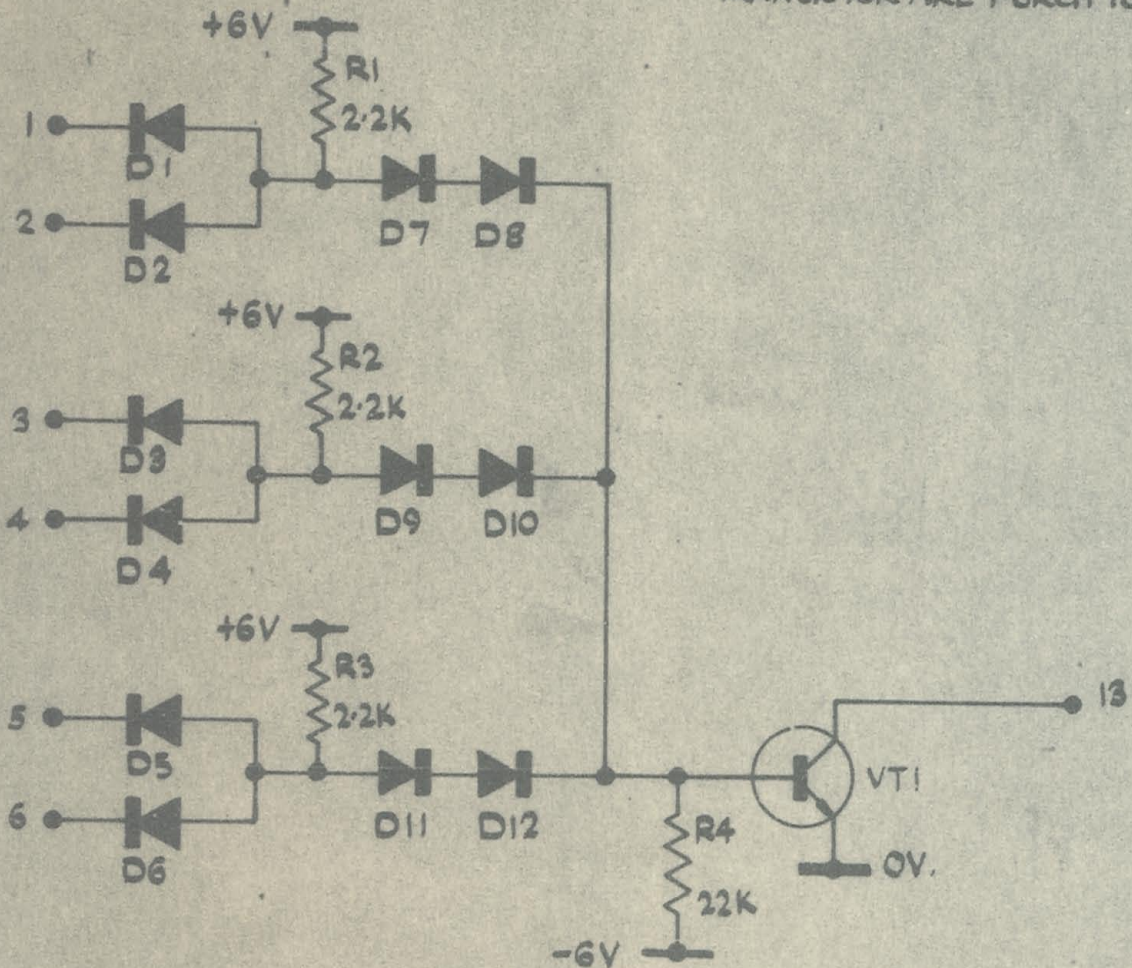
CONTROL MATRIX WAVEFORM AMPLIFIERS 920B

322 A7191

SHEET No 10
OF



DIODES ARE PURCH 101
TRANSISTOR ARE PURCH 100.

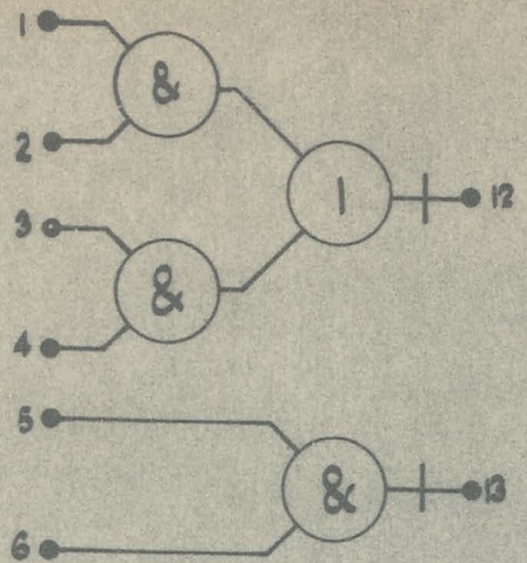
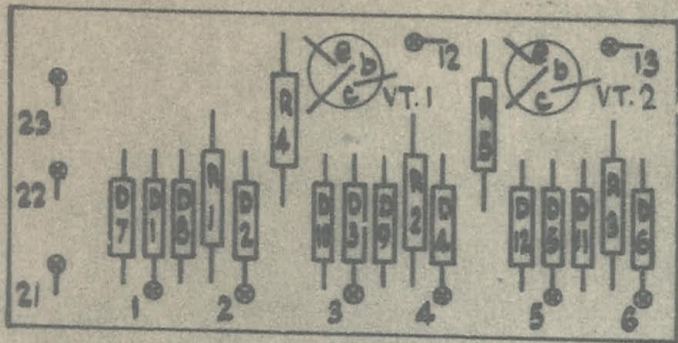


DRAWN	CAC.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPR VED	<i>Ed</i>	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

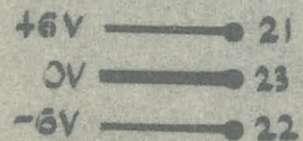
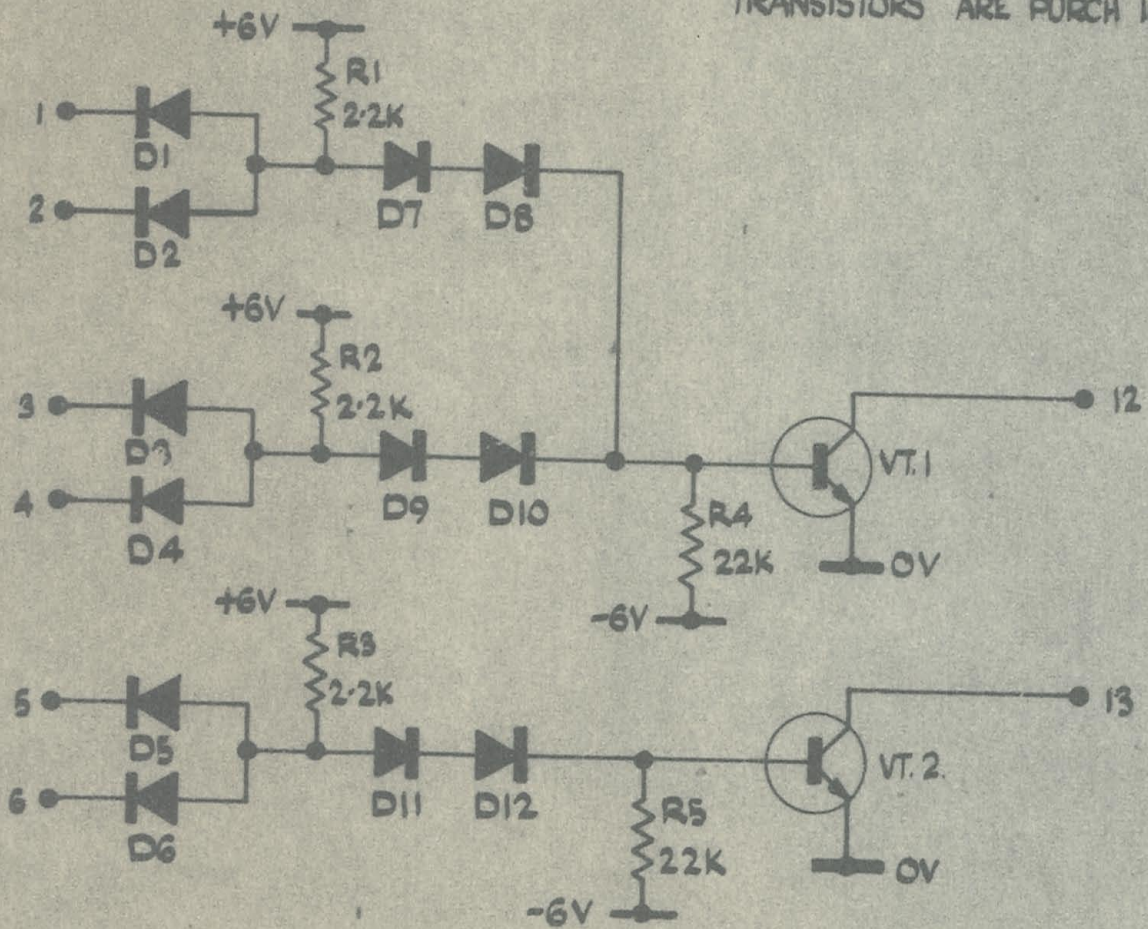
ELLIOTT BROTHERS (LONDON) LTD.

TITLE
L.S.A. 05
920B.

INSTRUCTION SHEET
322A 7191
SHEET No 11
OF



DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.



DRAWN	CAC.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
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DATE	16/5/66	INITIALS	C.A.C.

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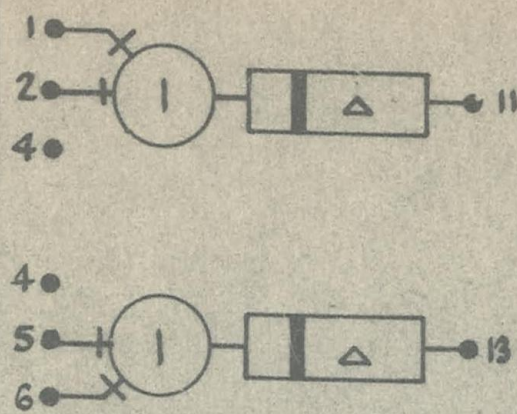
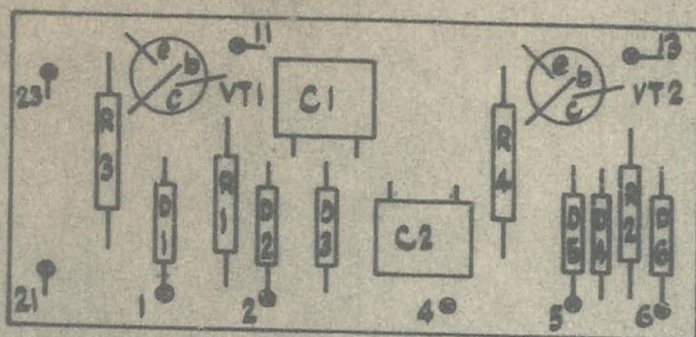
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L.S.A. 06
920 B

INSTRUCTION SHEET

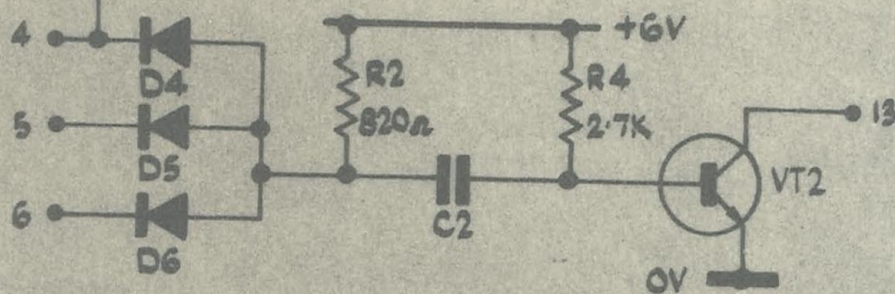
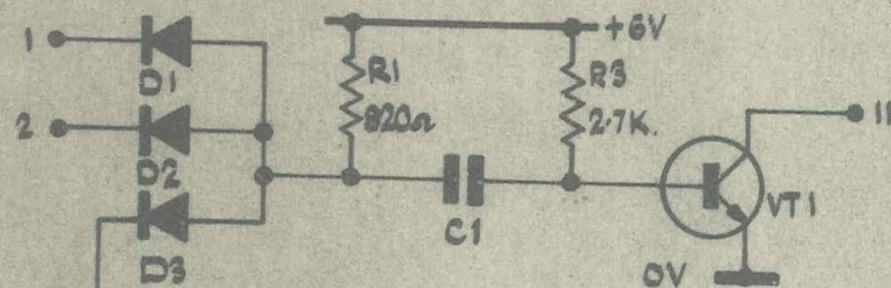
322A7191

SHEET No 12
OF



PULSE WIDTH (Δ) = $C \cdot R_s$ (WHERE C = CAPACITANCE IN pF.)

DIODES ARE PURCH 101,
TRANSISTORS ARE PURCH 100



+6V ——— 21
0V ——— 23

NOTE:-

PULSE WIDTH (+VE). PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN $N/2$ SEC. $1/p 4$ - 2.4V. REFERENCE VOLTAGE.

LSA. No.	C ₁	C ₂
07	100	100
13	330	330
34	100	330

DRAWN **C.A.C.** ISSUE No. **1** **2**
 CHECKED **CS** A.R. No. **1314** **1505**
 APPR'VED **E.H.H.** DATE **26-4-60** **29-6-66**
 DATE **16/5/60** INITIALS **C.A.C. R.W.C.**

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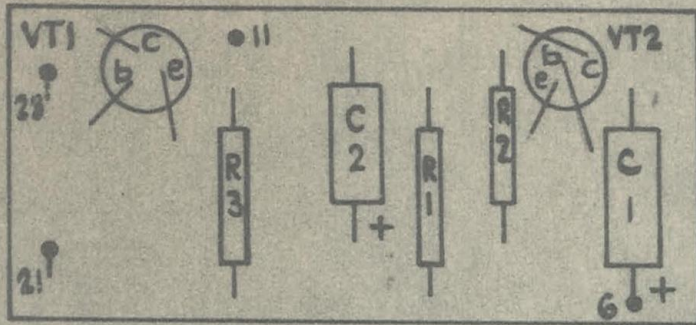
TITLE

L.S.A. 07, 13, 34
PULSE GENERATORS. 920B

INSTRUCTION SHEET

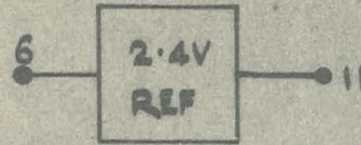
322A 7191

SHEET No 13
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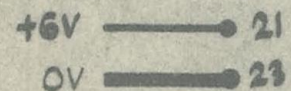
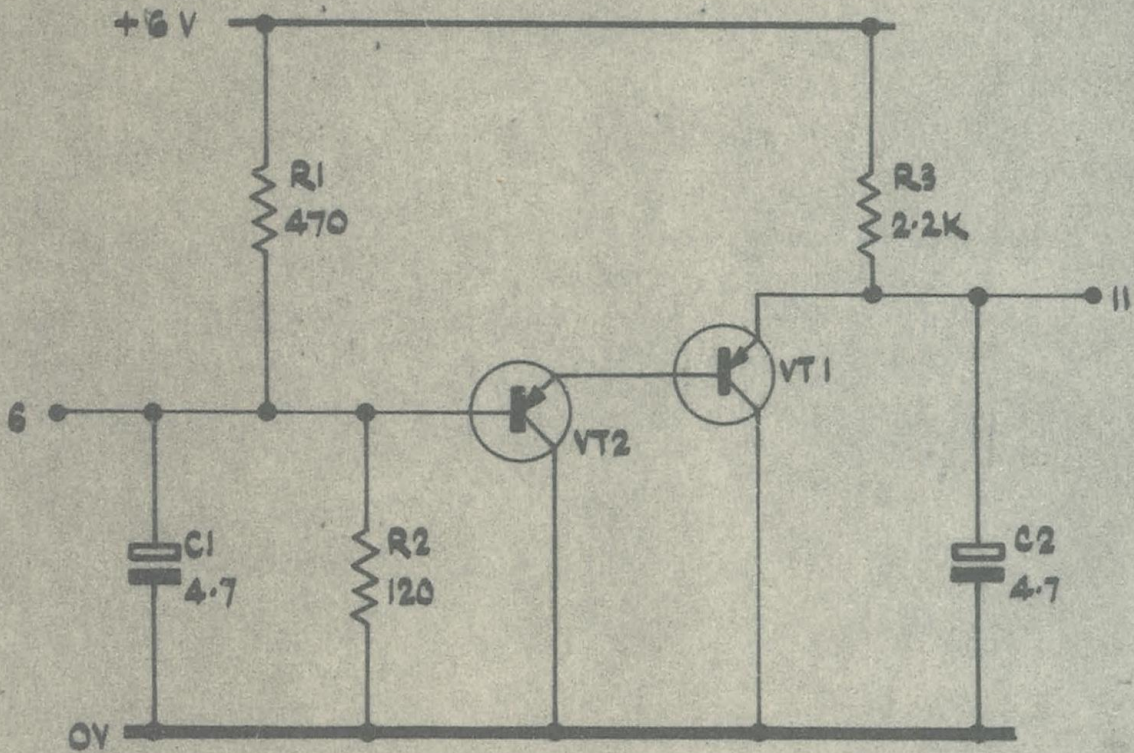


I/P 6 VARIES O/P 11 VOLTAGE FOR MARGINAL TEST.

O/P 11 PROVIDES 2.4V REF.



TRANSISTORS ARE MM 2712



DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1374	1505
APPROVED	<i>[Signature]</i>	DATE	26-4-66	29-6-66
DATE	16/5/66	INITIALS	C.A.C.	C.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

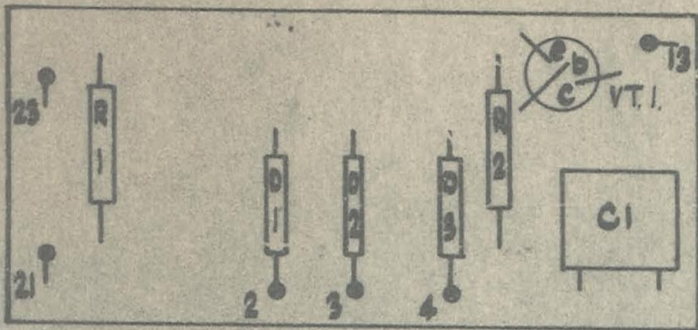
TITLE

L.S.A. 08
VOLTAGE REFERENCE 9208

INSTRUCTION SHEET

322A 7191

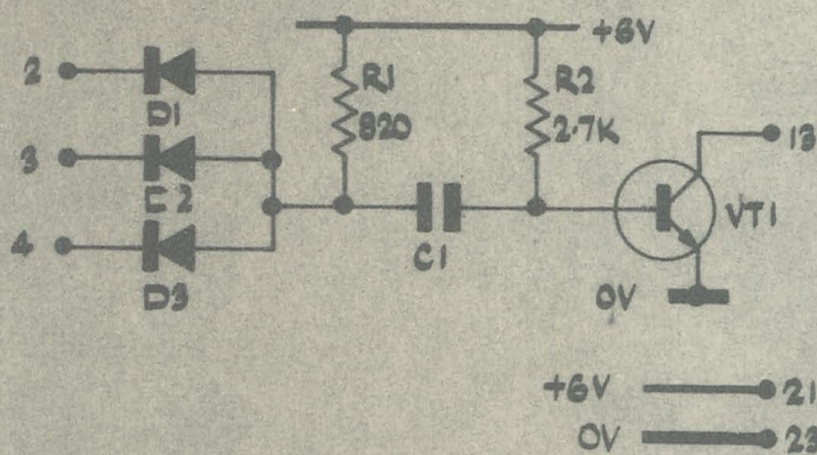
SHEET No 14
OF



PULSE WIDTH (Δ) = $C \tau_s$ (WHERE
 C = CAPACITANCE IN pF)

DIODES ARE PURCH 101.
 TRANSISTORS ARE PURCH 100.

LSA. No.	C1
09	470
14	680



NOTE:-

PULSE WIDTH (+VE), PULSE TRIGGERED BY ANY INPUT
 REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1'
 FOR $> \frac{N}{3}$ SEC.

I/P 4 - 2.4V REFERENCE VOLTAGE.

DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1374	1505
APPROVED	S.M.	DATE	26-4-66	29-6-66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

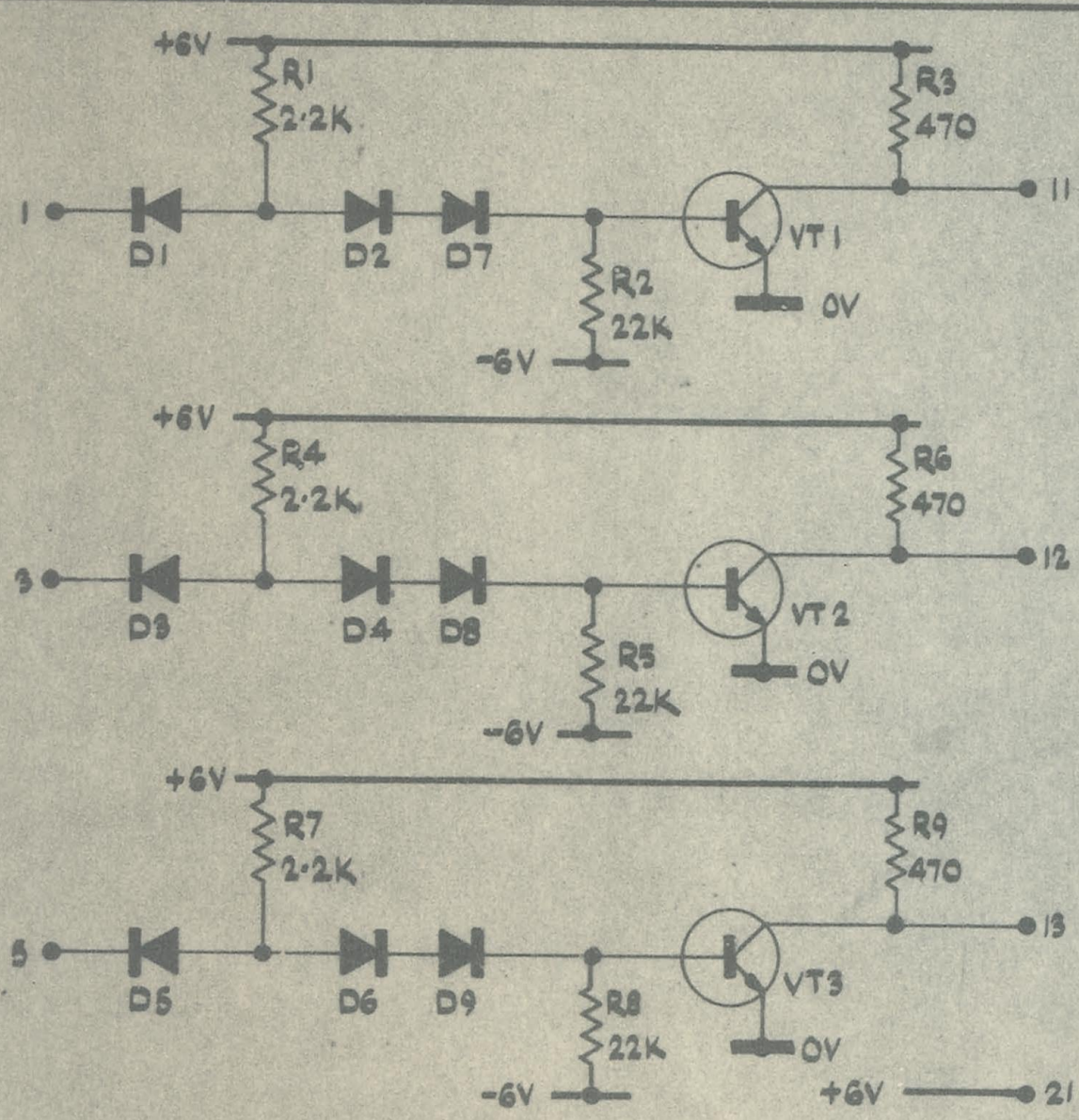
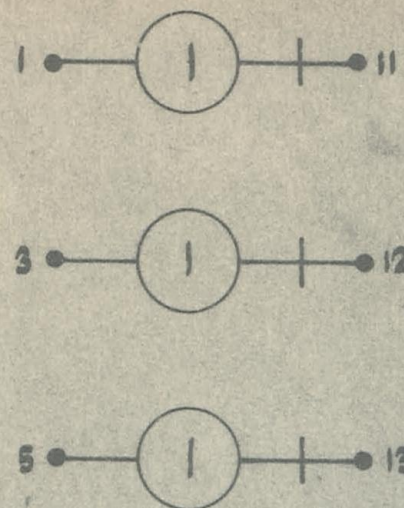
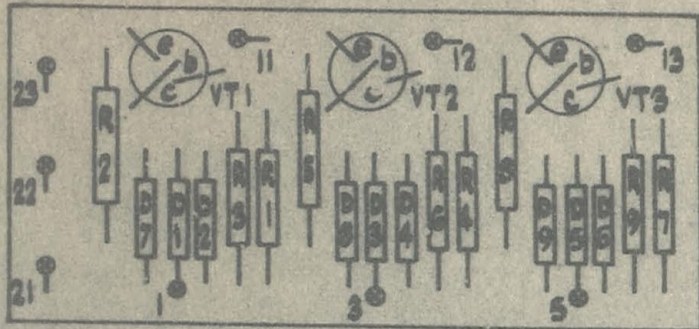
TITLE

L.S.A. 09, 14,
 PULSE GENERATOR, 920B

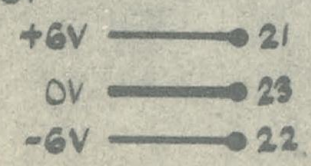
INSTRUCTION SHEET

322A 7191

SHEET No 15
 OF



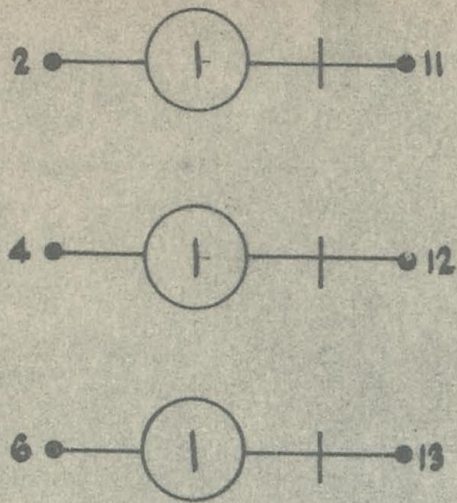
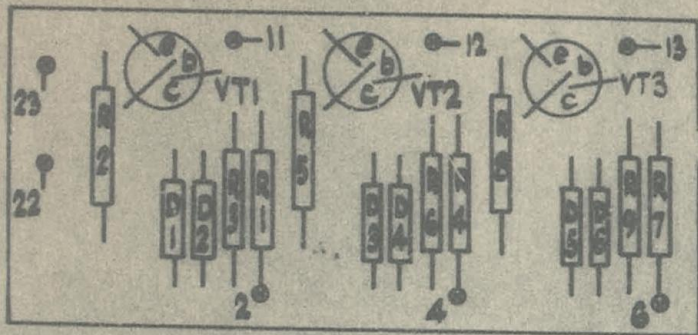
DIODES ARE PURCH 101.
TRANSISTORS ARE PURCH 100.



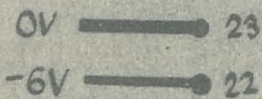
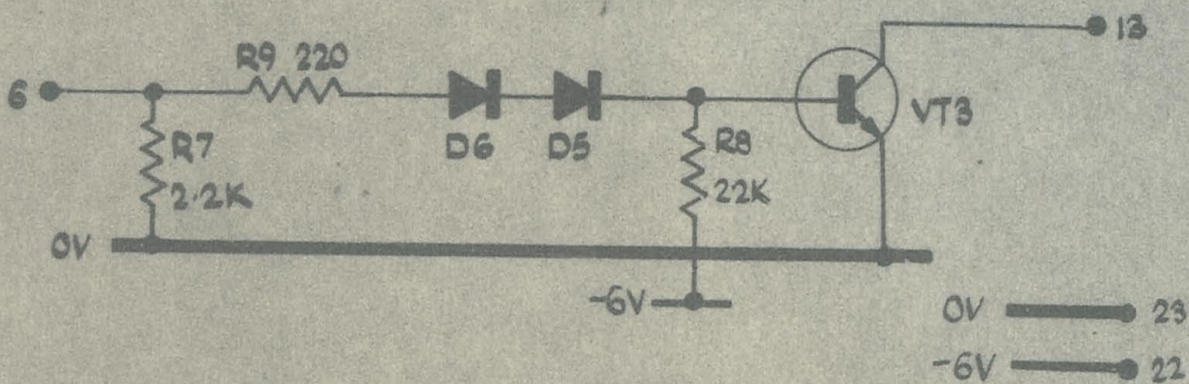
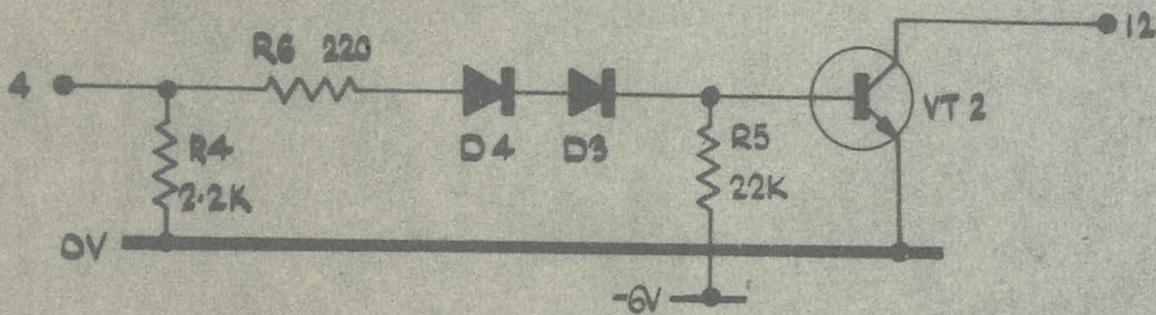
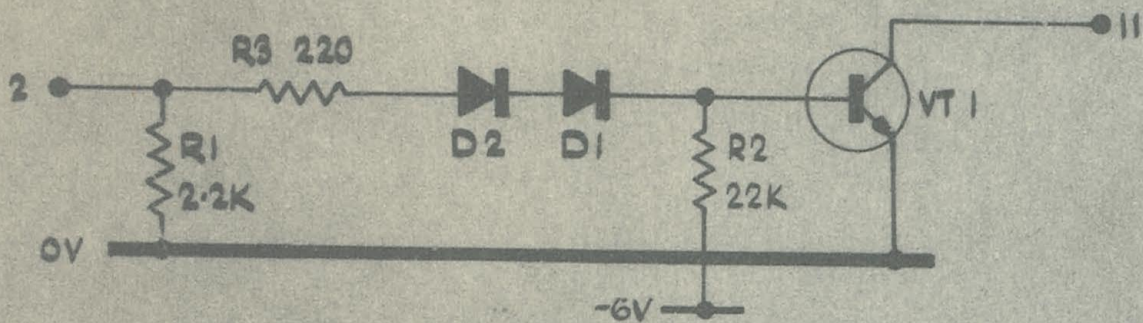
DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPR VED	R.L.	DATE	26-1-66
DATE	16/5/62	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE	L.S.A. II CABLE TRANSMITTERS '9208	INSTRUCTION SHEET	322A7191
			SHEET No 16 OF



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100



DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS458	A.R. No.	1374
APPROVED	<i>[Signature]</i>	DATE	25-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

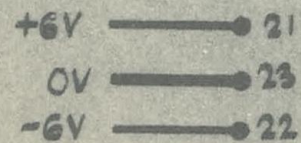
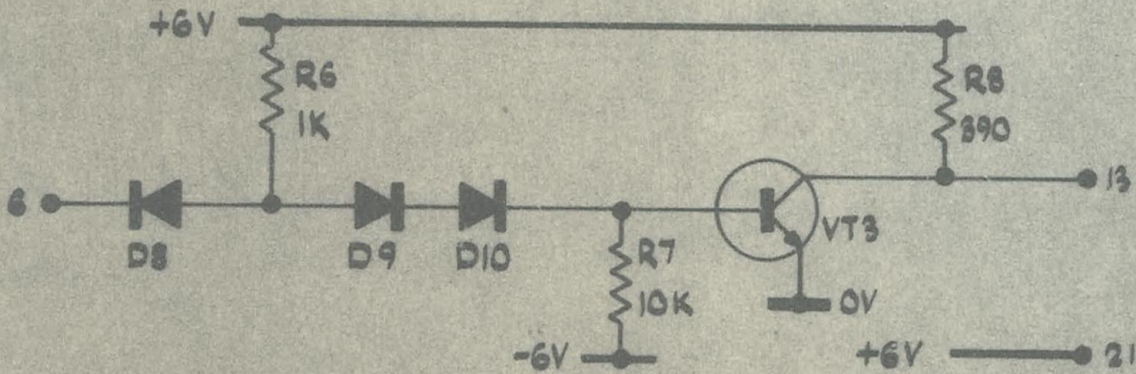
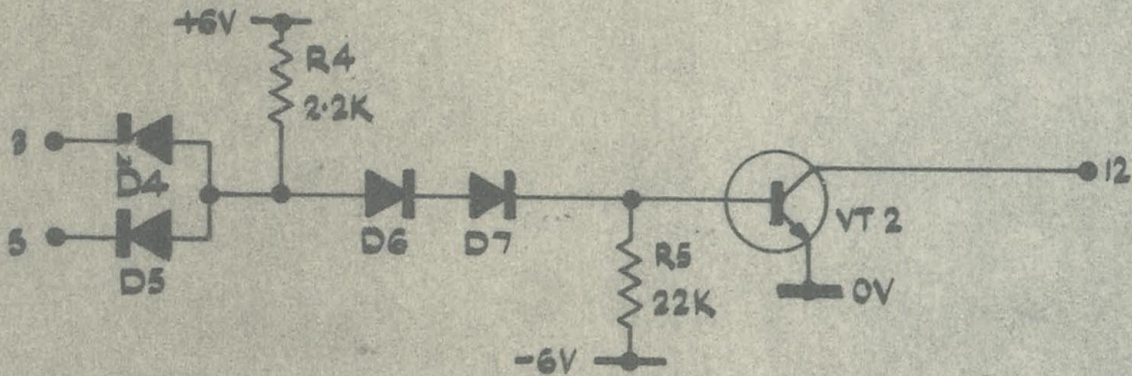
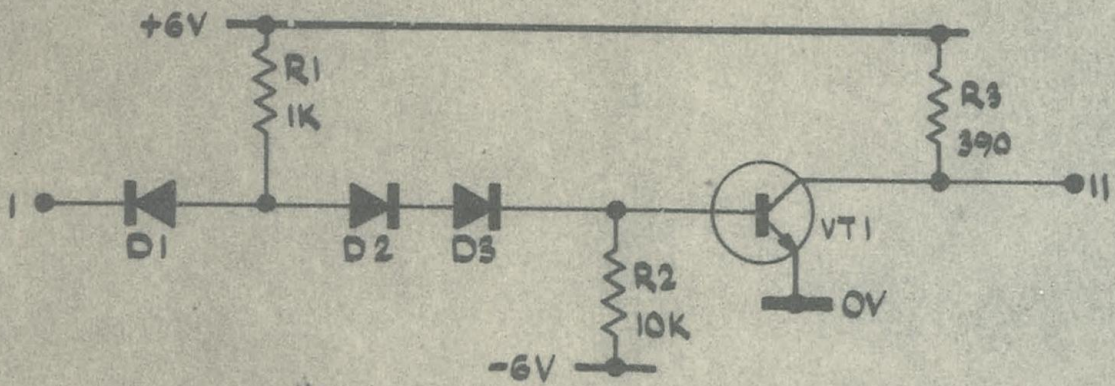
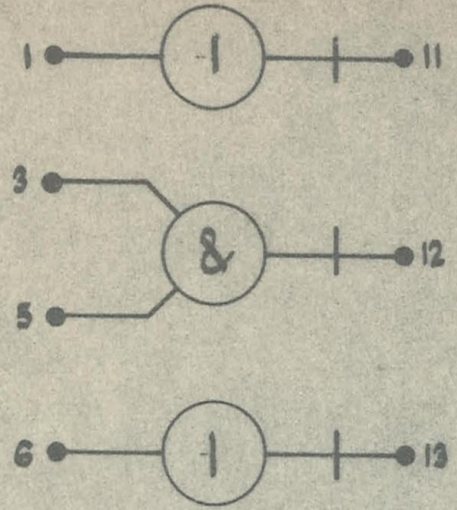
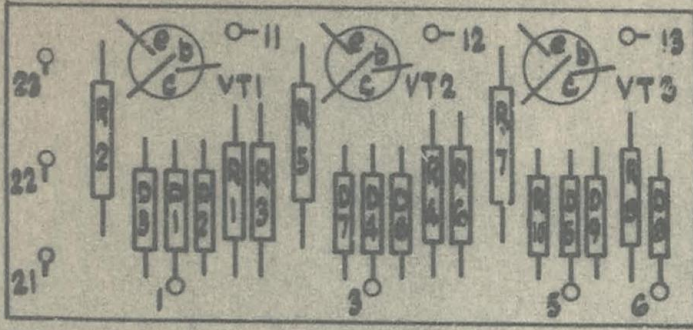
TITLE

L.S.A. 12.
CABLE RECEIVERS 920B

INSTRUCTION SHEET

322A 7191

SHEET No 17
OF



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPR VED	S.M.	DATE	26-4-66
DATE	14/5/66	INITIALS	C.A.C.

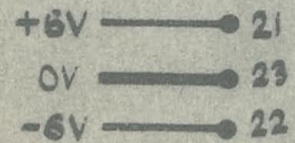
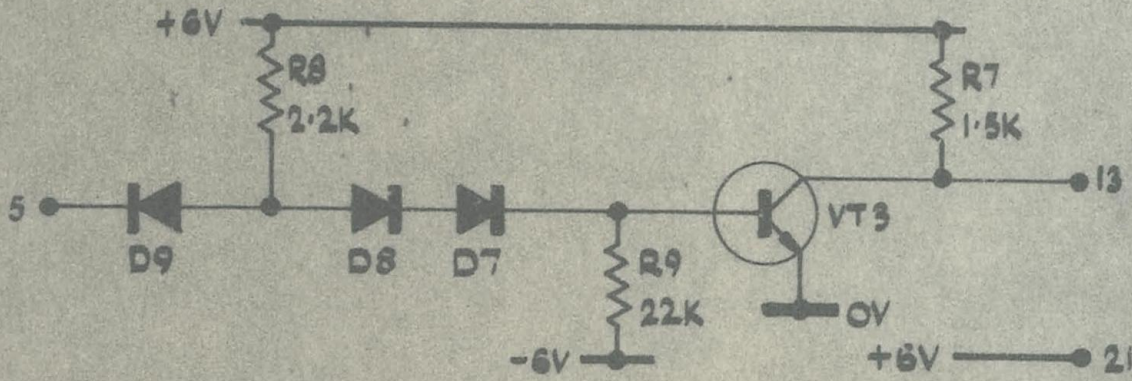
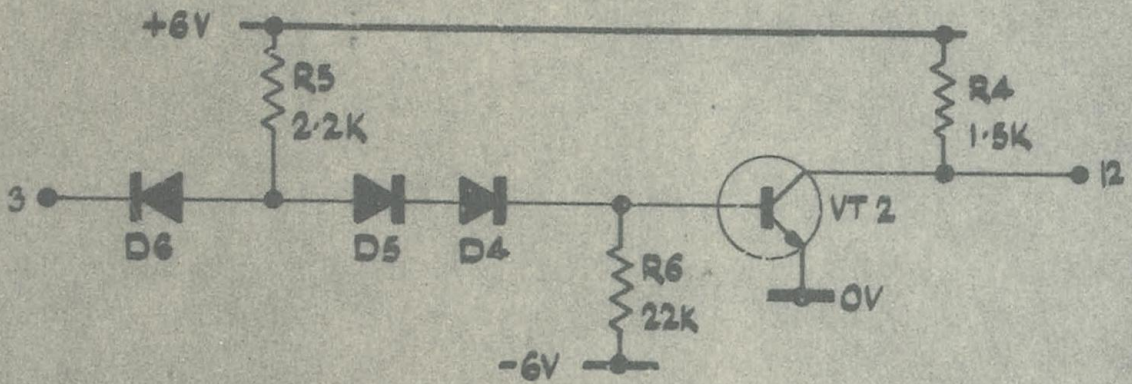
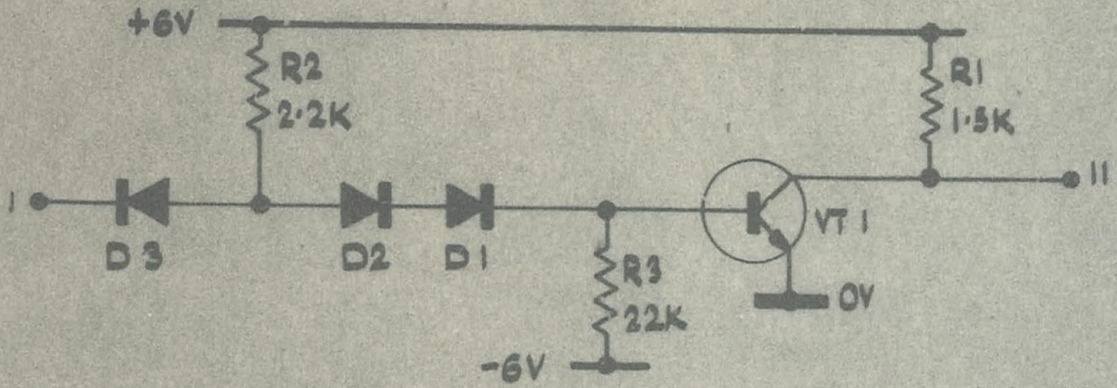
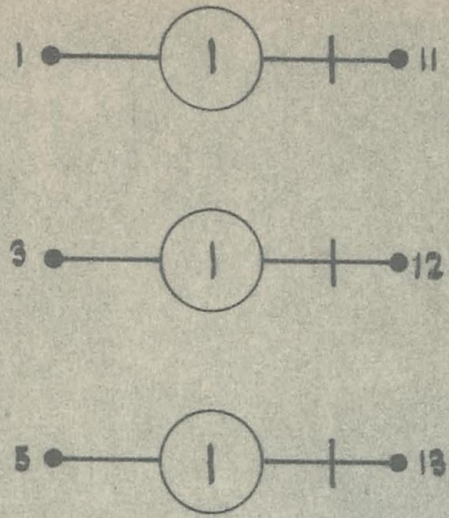
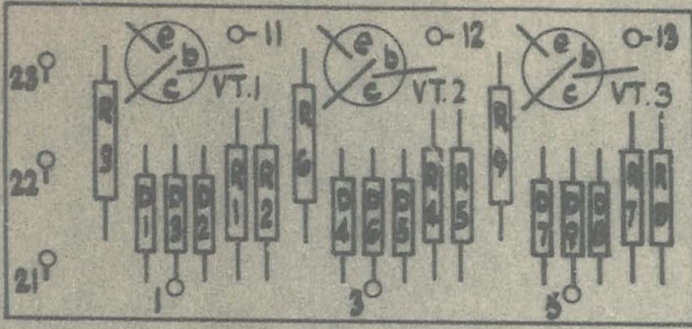
ELLIOTT BROTHERS (LONDON) LTD.

TITLE: L.S.A. 15 920B
2-INPUT NAND GATE + 2 INVERTING DRIVERS

INSTRUCTION SHEET

322A7191

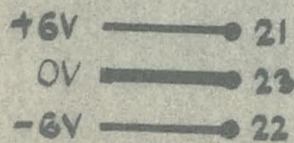
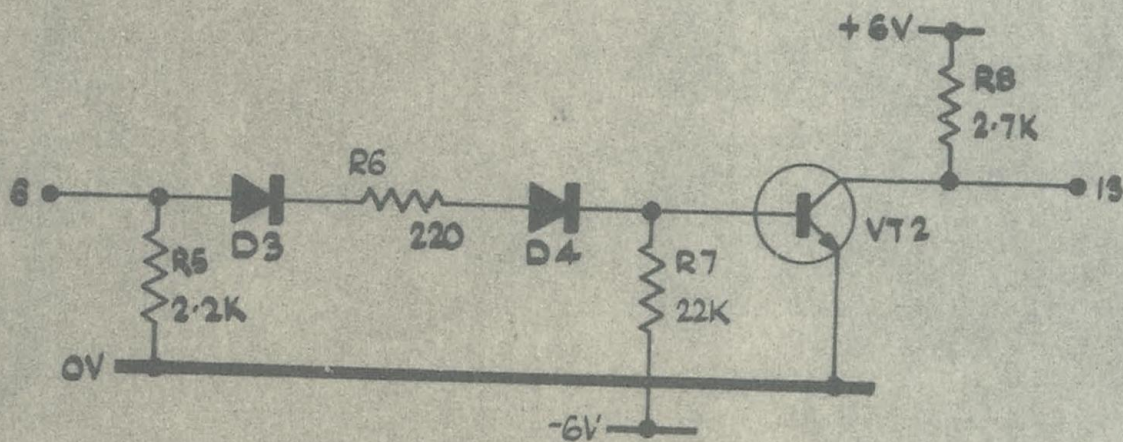
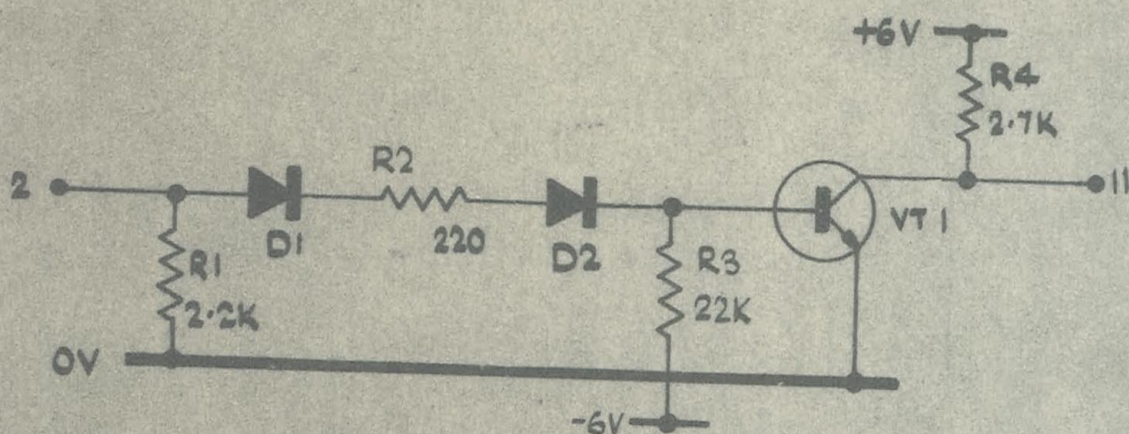
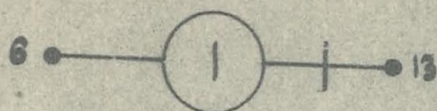
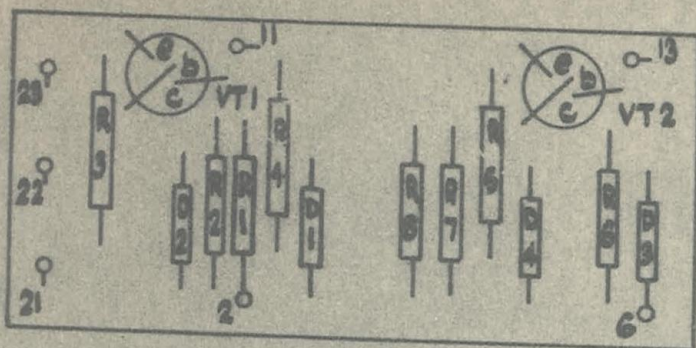
SHEET No 18 OF



DIODES ARE PURCH 101
 TRANSISTORS ARE PURCH 100.

DRAWN C.A.C.	ISSUE No. 1
CHECKED CS456	A.R. No. 1374
APPROVED <i>[Signature]</i>	DATE 26-4-66
DATE 16/5/66	INITIALS C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.



DIODES ARE PURCH 101
 TRANSISTORS ARE PURCH 100.

DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1374	1505
APPROVED	<i>[Signature]</i>	DATE	26-4-66	29-6-66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

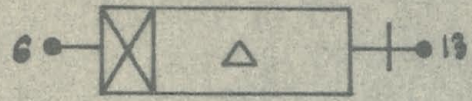
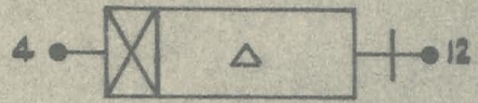
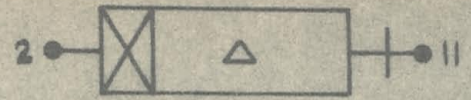
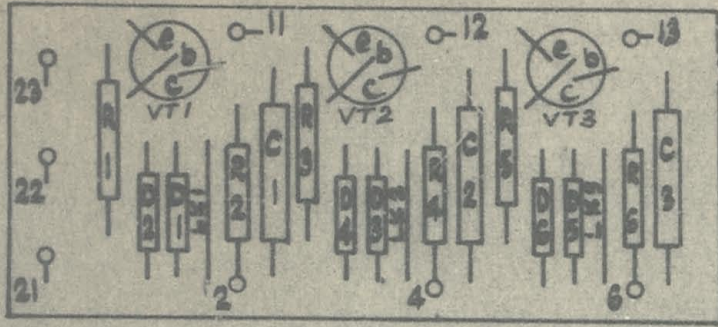
TITLE

L.S.A. 17.
 PAPER TAPE RECEIVER 9208.

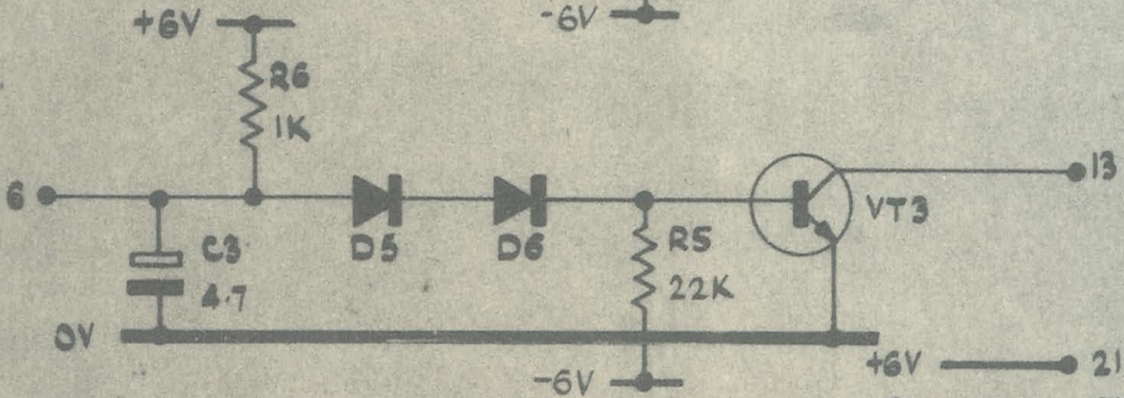
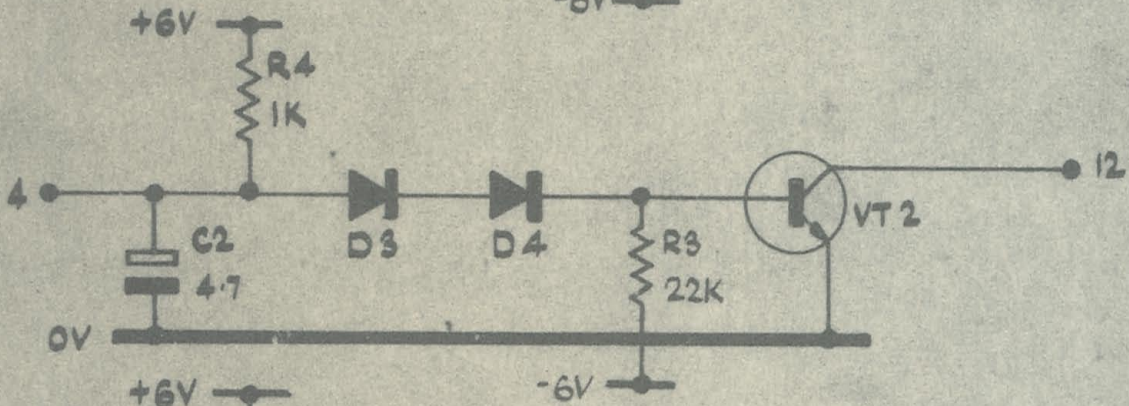
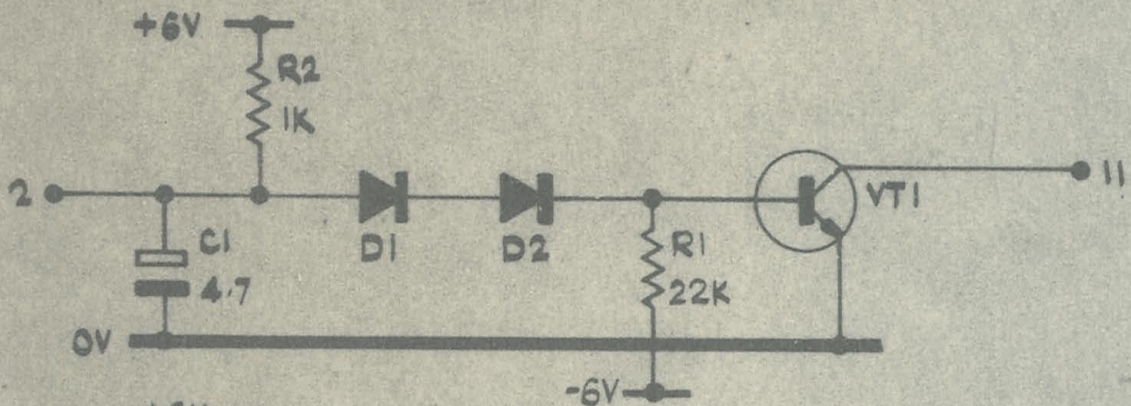
INSTRUCTION SHEET

322A 7191

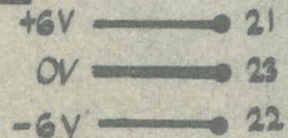
SHEET No 20
 OF



$\Delta \approx 1ms$



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100



DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1374	1505
APPR VED	R.M.	DATE	26-4-66	29-6-66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.

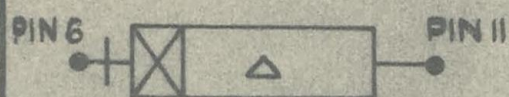
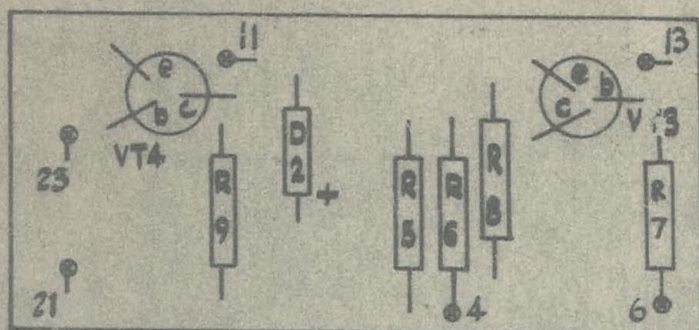
ELLIOTT BROTHERS (LONDON) LTD.

TITLE
L.S.A. 18.
SINGLE I/P NOISE REJECTION INVERTER. 9208

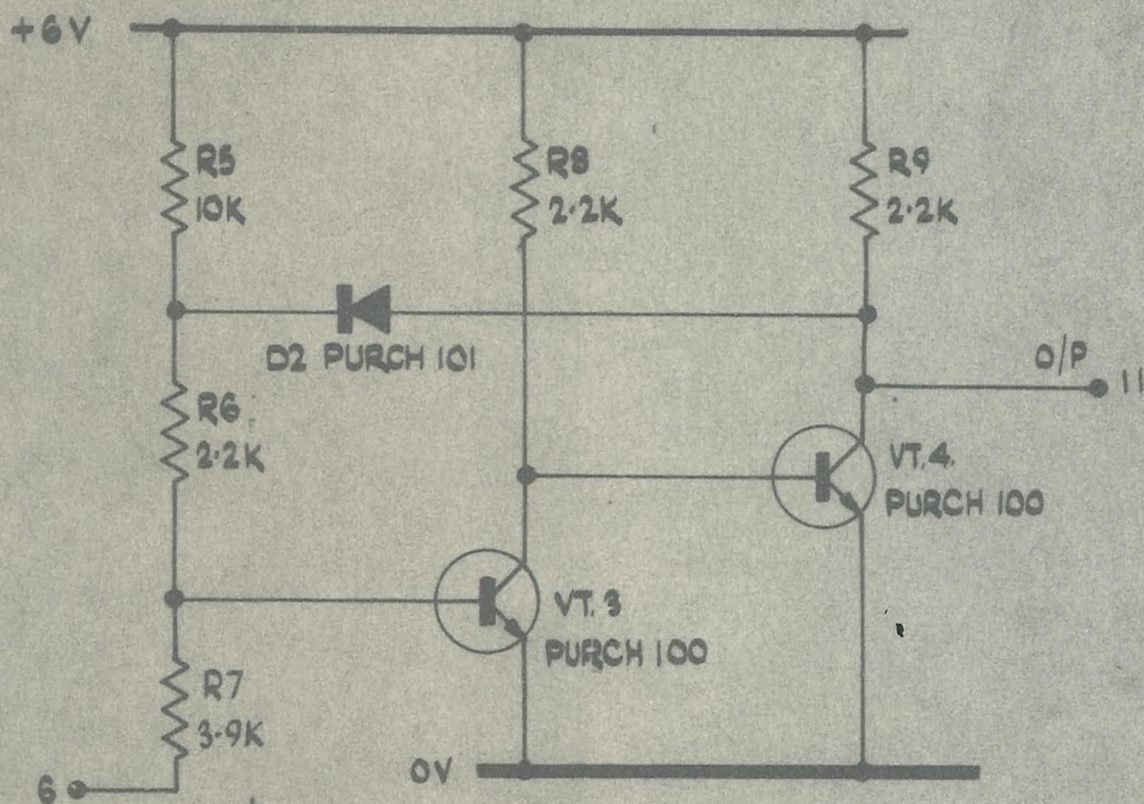
INSTRUCTION SHEET

322A7191

SHEET No 21
OF



ONLY USED FOLLOWING LSA. 20 OR 21. COMBINATION CIRCUIT GIVES DELAY (Δ) $\approx 10\text{ms}/\mu\text{F}$ WHERE μF IS CAPACITANCE OF LSA 20 OR LSA 21.



DIODE IS PURCH 101
TRANSISTORS ARE PURCH 100

+6V ——— 21
0V ——— 23

DRAWN	C.A.C.	ISSUE No.	1	2				
CHECKED	CS 456	A.R. No.	1374	1505				
APPROVED	<i>[Signature]</i>	DATE:	26-4-66	8-7-66				
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.				

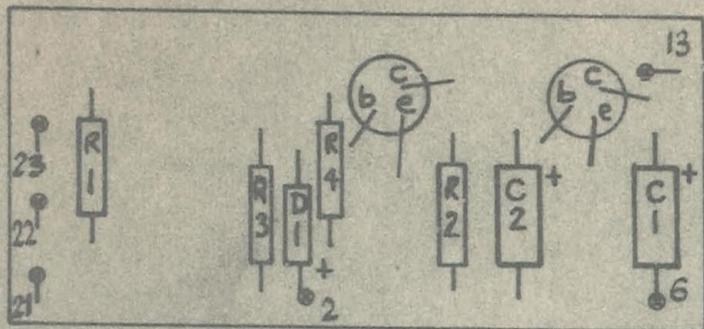
ELLIOTT BROTHERS (LONDON) LTD.

L.S.A. 19
DELAY 920B

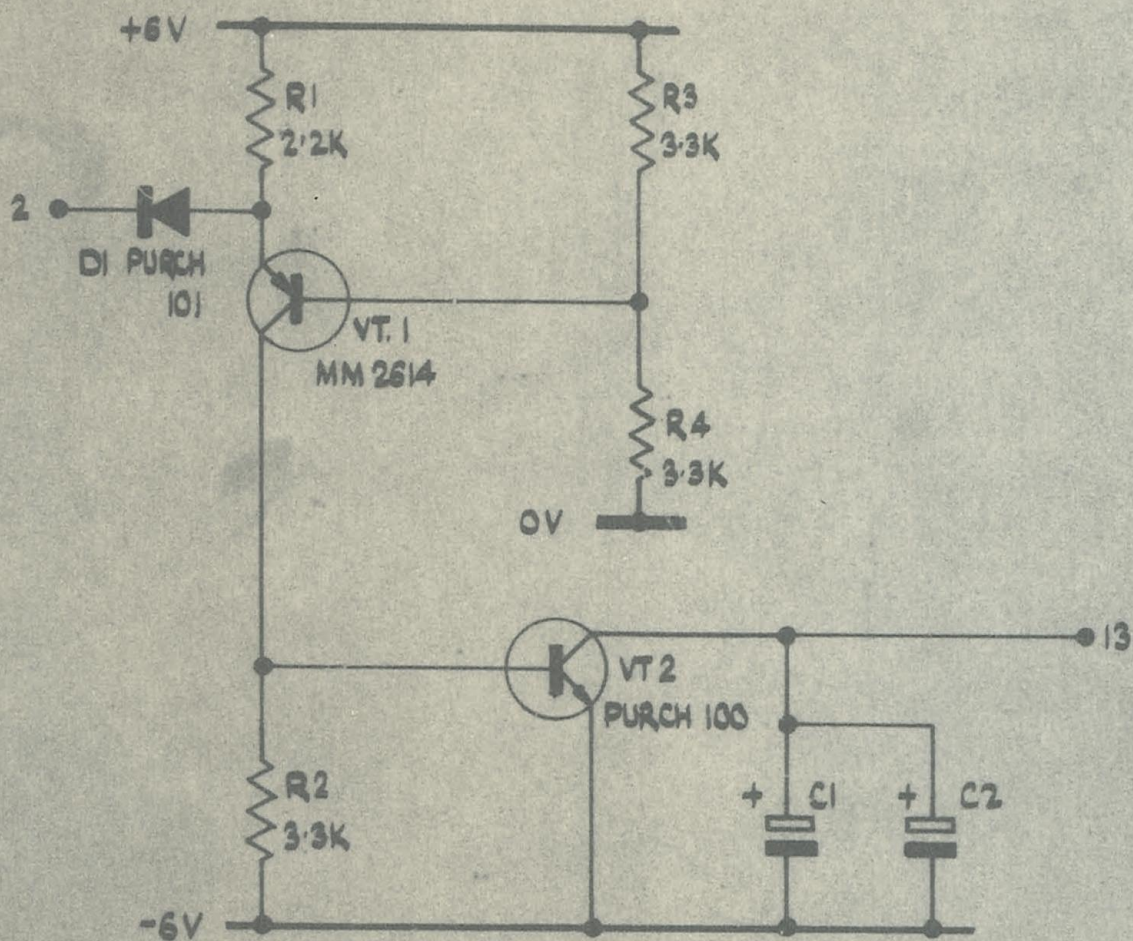
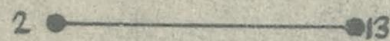
INSTRUCTION SHEET

322A7191

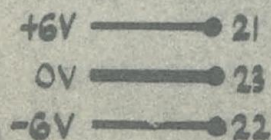
SHEET No 22
OF



ONLY USED PRECEDING L.S.A.
 19. OVERALL DELAY $\approx 10 \text{ ms}/\mu\text{F}$
 WHERE μF IS CAPACITANCE OF
 $C_1 + C_2$



ELEMENT	C1	C2
LSA 20	4.7 μF	4.7 μF
LSA 24	2.2 μF	1.0 μF
LSA 25	2.2 μF	0.047 μF



DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1374	1505
APPROVED	S.M.	DATE	26-4-66	6-66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

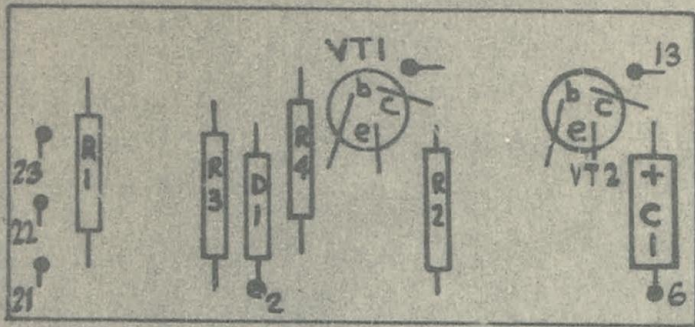
TITLE

L.S.A. 20, 24, 25.
 DELAY.

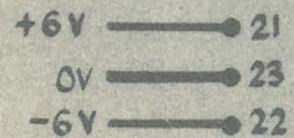
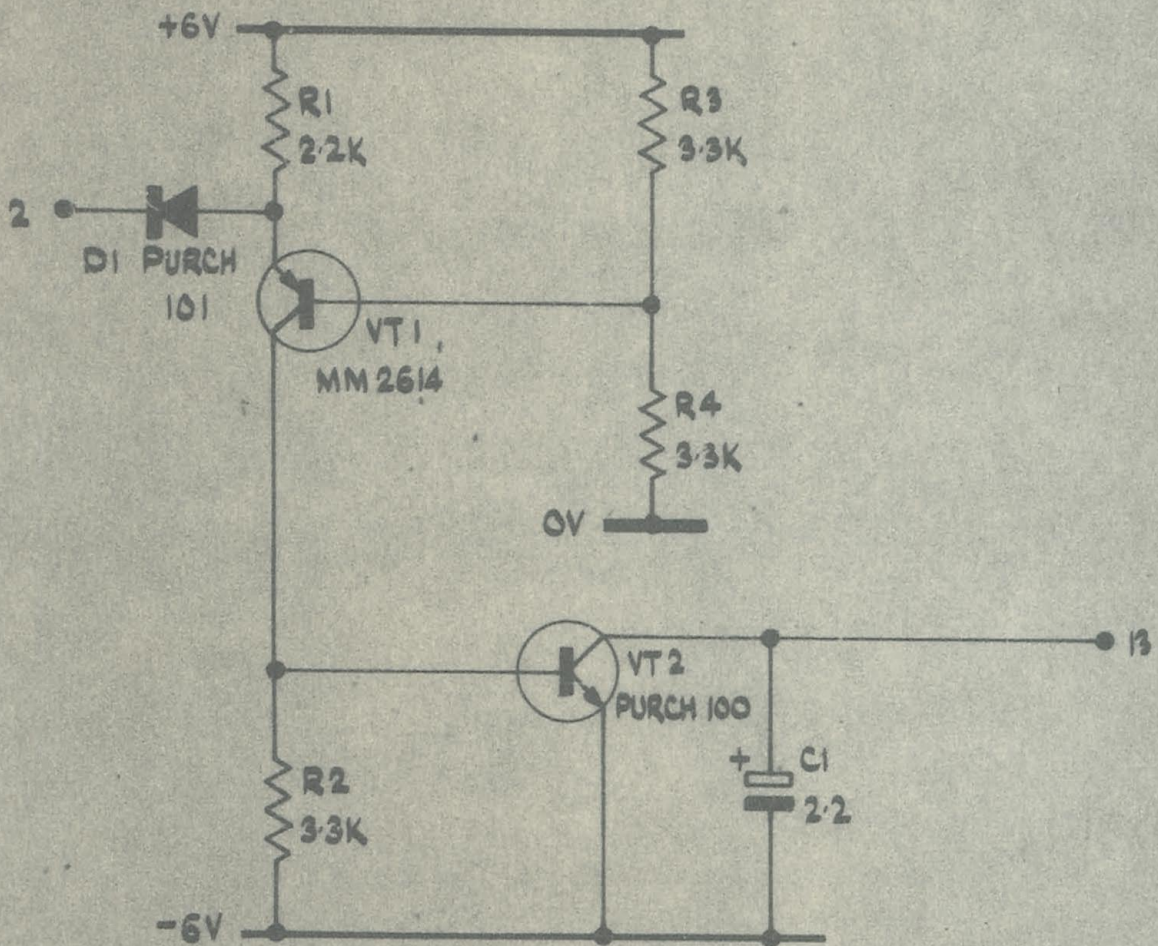
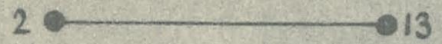
INSTRUCTION SHEET

322A 7191

SHEET No 23
 OF



ONLY USED PRECEEDING L.S.A
 19. OVERALL DELAY $\approx 10 m\mu F$
 WHERE μF IS CAPACITANCE OF
 C1



DRAWN	C.A.C.	ISSUE No.	1	2						
CHECKED	C3456	A.R. No.	1374	1505						
APPROVED	<i>[Signature]</i>	DATE	26-4-66	29-6-66						
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.						

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

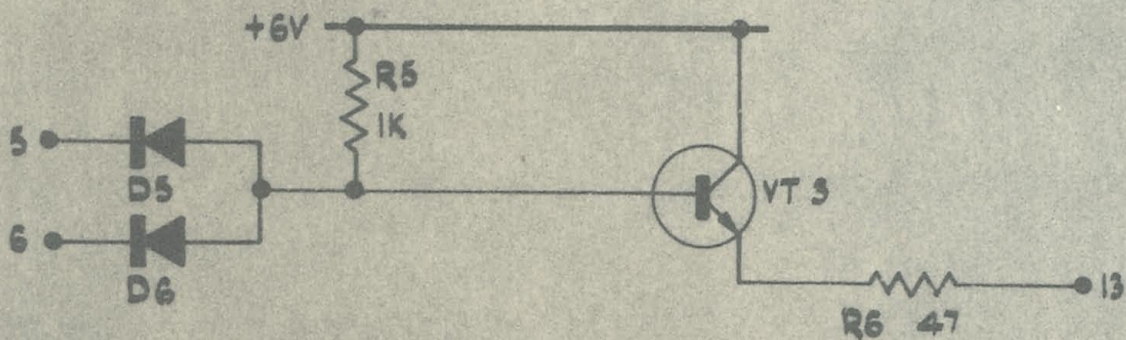
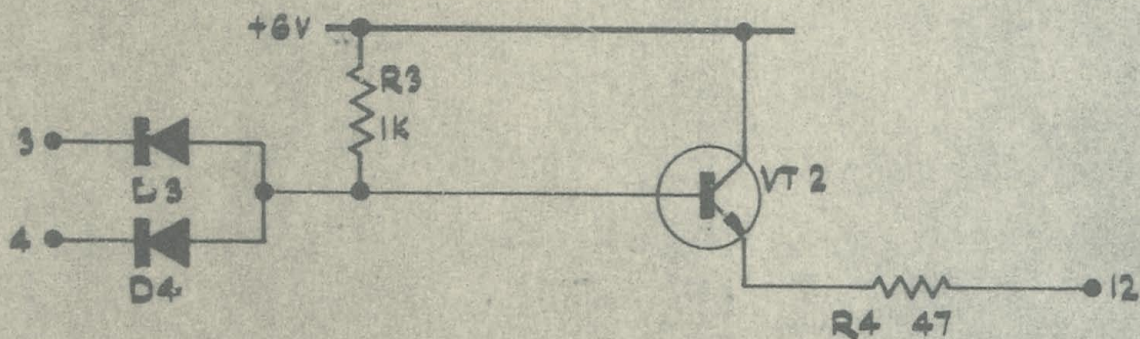
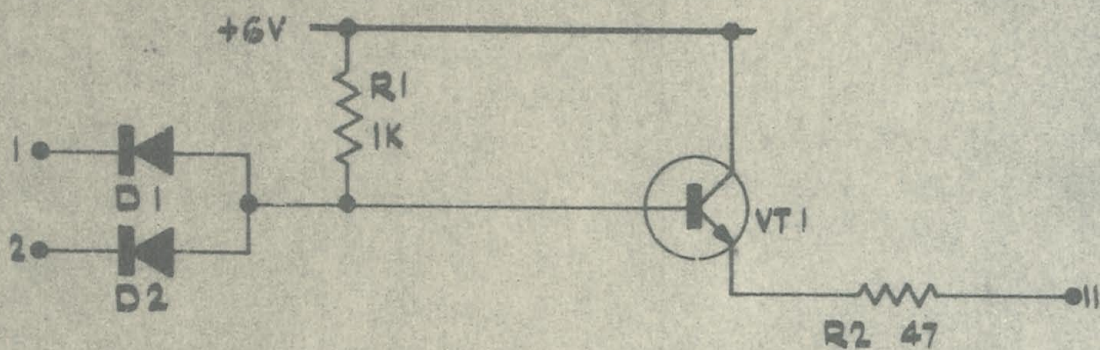
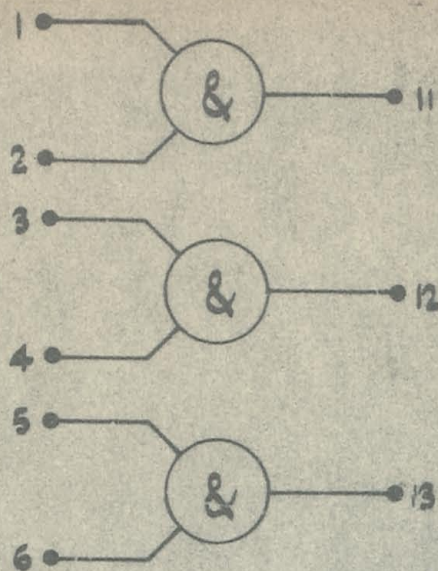
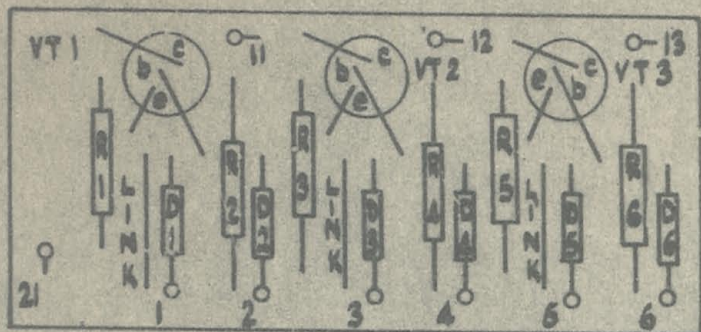
L.S.A. 21.
 DELAY.

INSTRUCTION SHEET

322A7191

SHEET No 24
 OF

O/P'S 11, 12, 13, TO 50 Ω COAX.



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100

+6V ———> 21

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPROVED	<i>[Signature]</i>	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

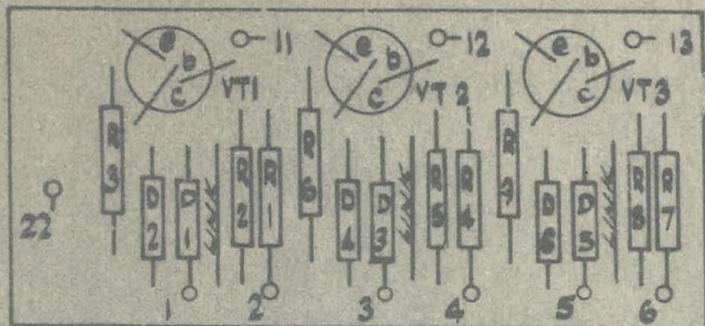
TITLE

L.S.A. 22.
TWO INPUT TRANSMITTERS.

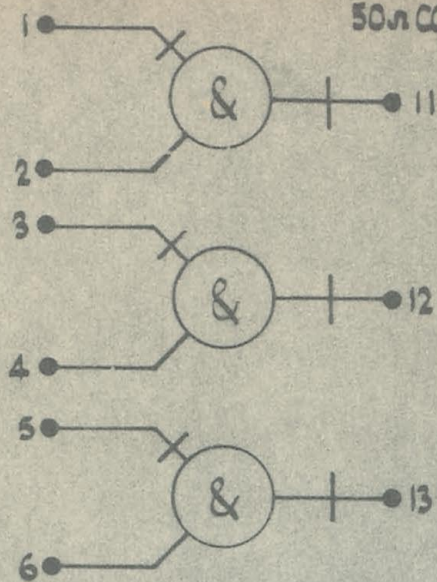
INSTRUCTION SHEET

322 A 7191

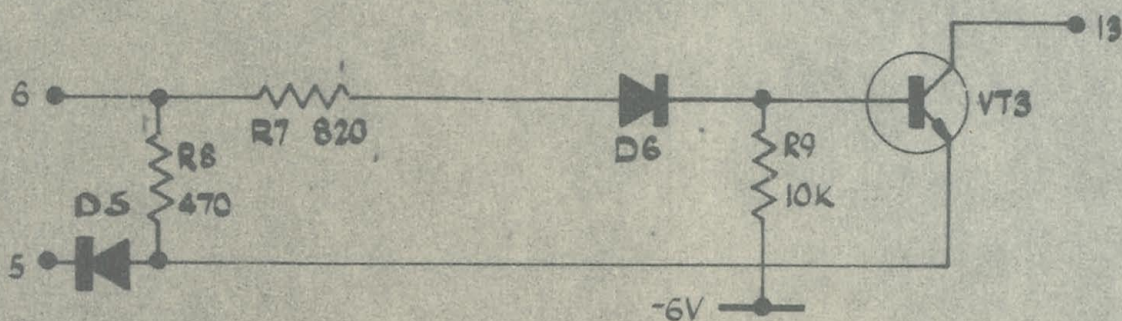
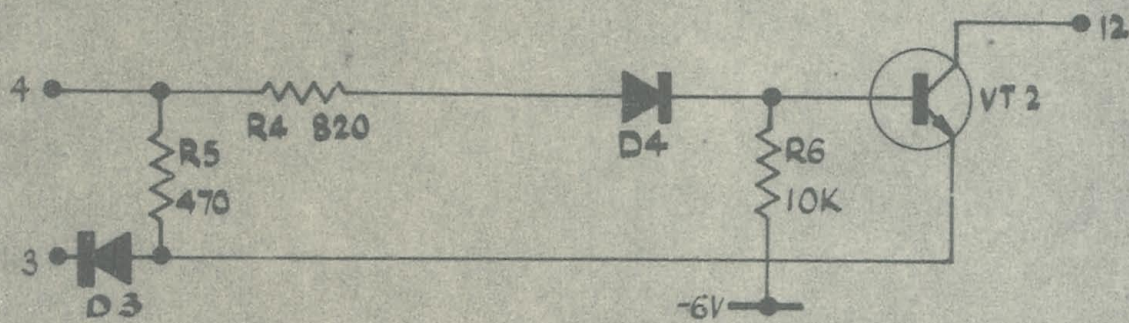
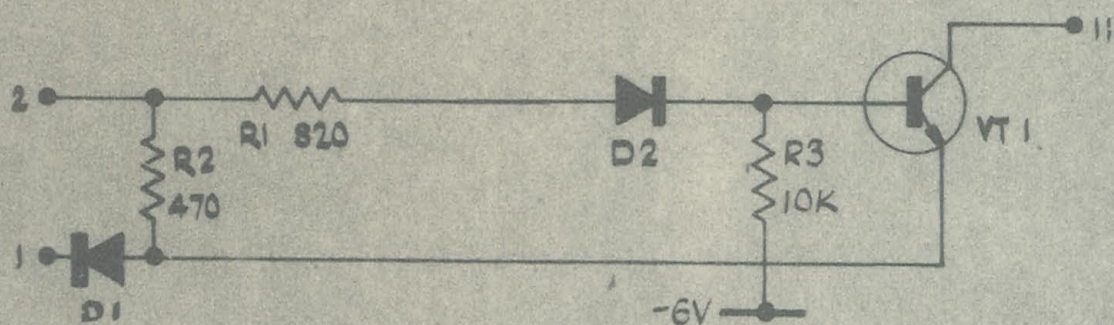
SHEET No 25
OF



I/P'S 2, 4, 6. - DATA INPUTS FROM
50Ω COAX



I/P'S 1, 3, 5. CONNECTED TO AN
O/P OF AN LSA 28.



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100

-6V ——— 22

DRAWN	C.A.C.	ISSUE No	1 2
REVISED	CS 456	PAR No	1374 1796
APPROVED	Z.R.V.	DATE	26-4-66 26/1/66
	16/5/66	INITIAL	C.A.C.

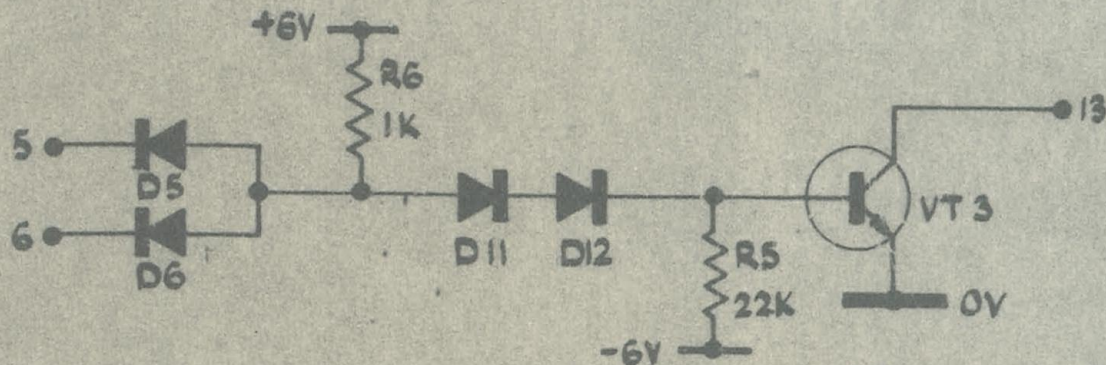
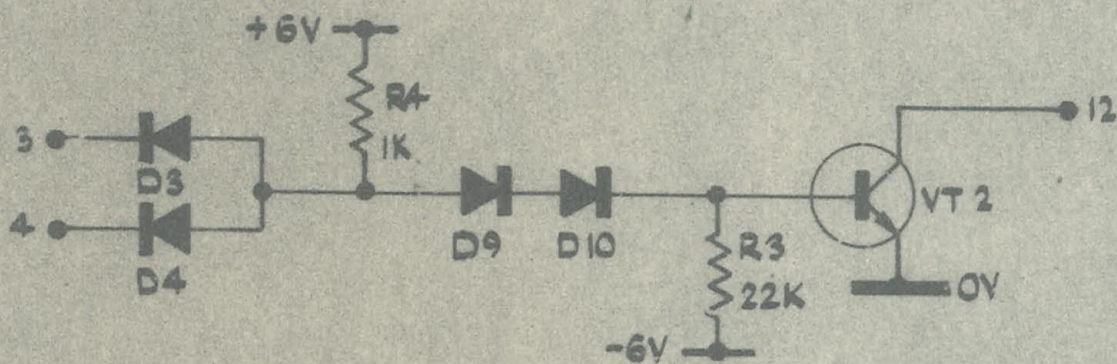
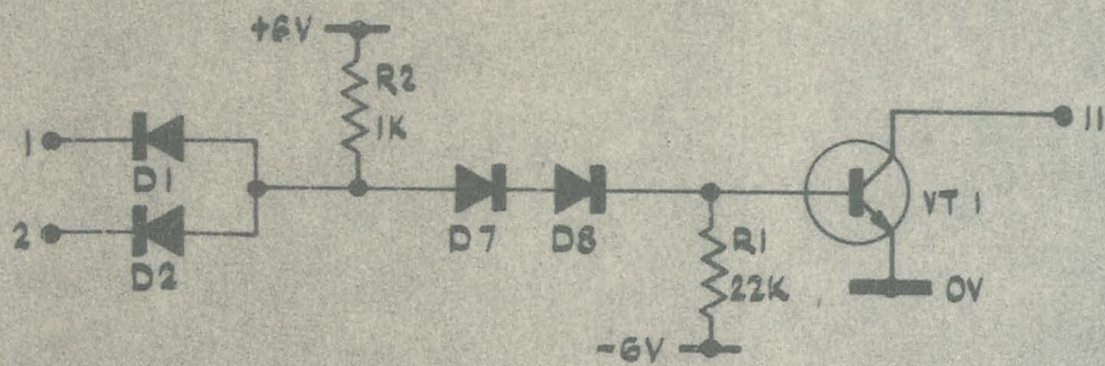
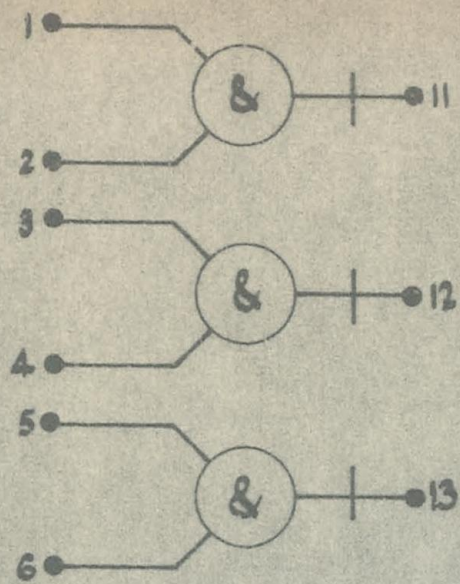
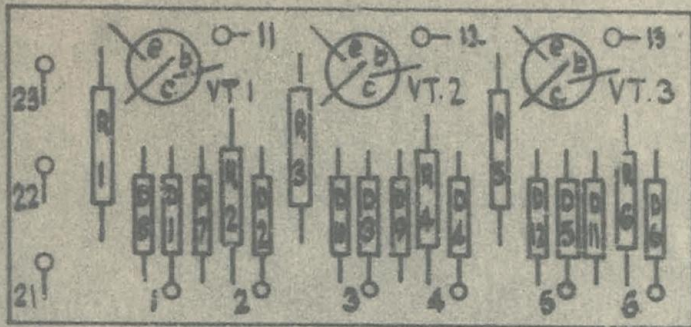
ELLIOTT BROTHERS (LONDON) LTD.

L.S.A. 23
GATED RECEIVERS.

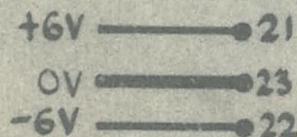
INSTRUCTION SHEET

322 A 7191

SHEET No 26
OF



DIODES ARE PURCH 101
TRANSISTORS ARE PURCH 100.



DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPROVED	<i>[Signature]</i>	DATE	25-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

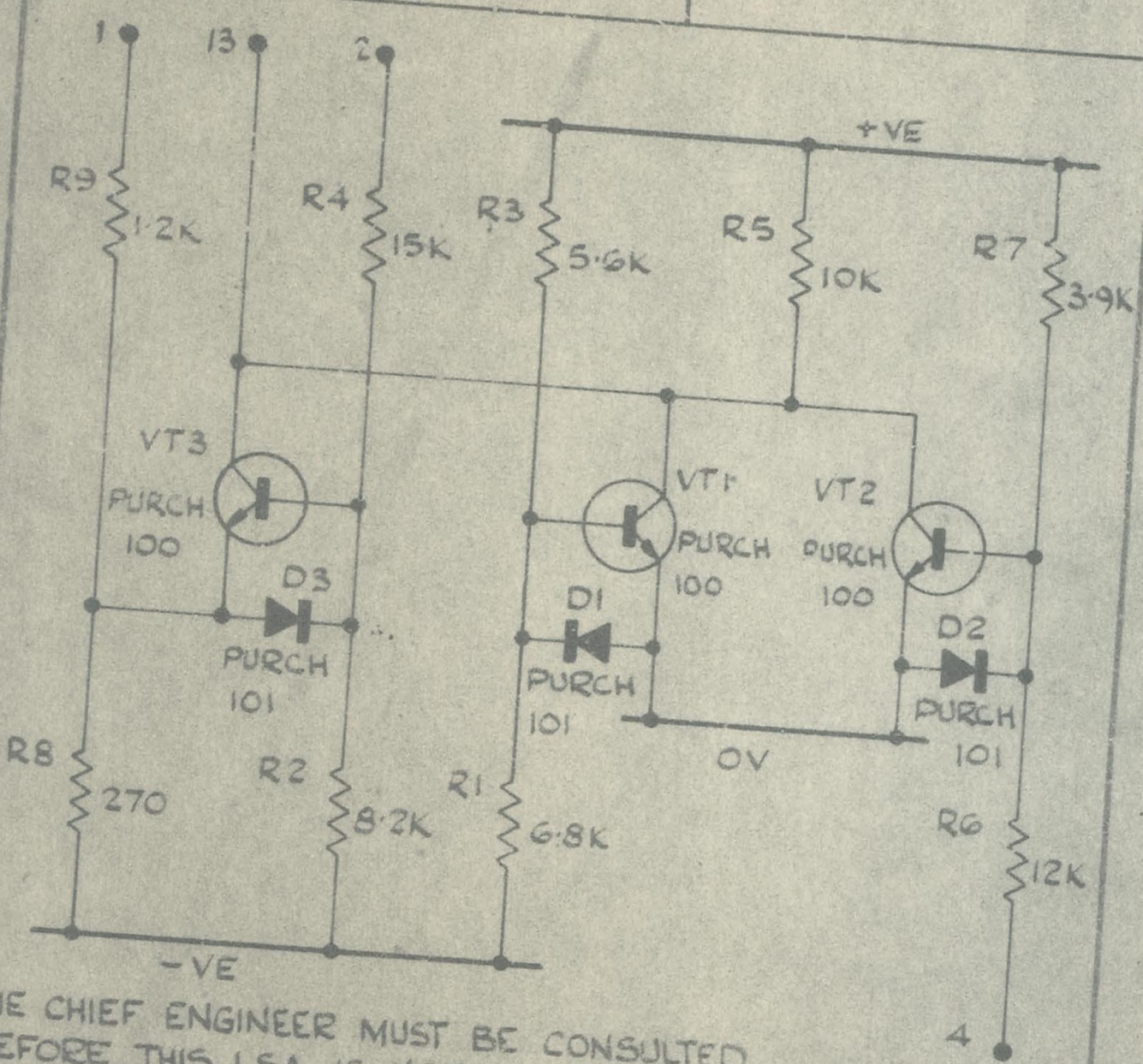
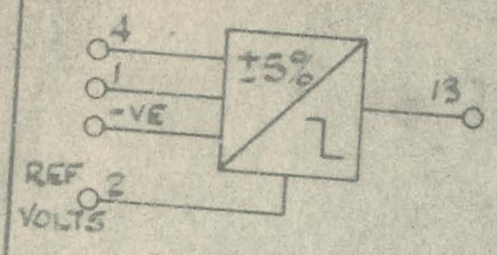
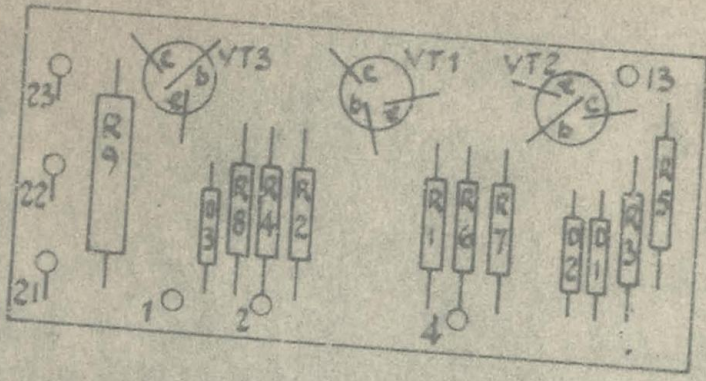
STYLE

L.S.A. 28
2-INPUT NAND GATES.

INSTRUCTION SHEET

322A7191

SHEET No 27
OF



THE CHIEF ENGINEER MUST BE CONSULTED BEFORE THIS LSA IS USED ON ANY PROJECT OTHER THAN THE MARITIME STORE.

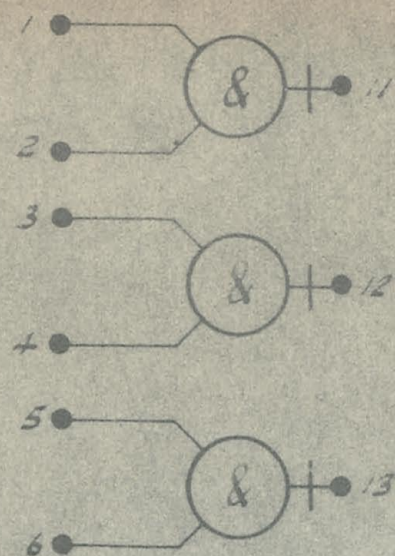
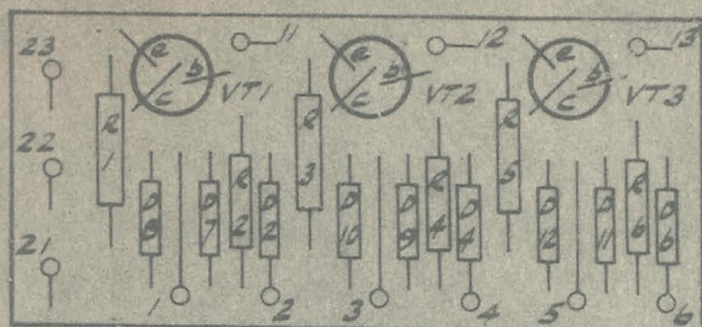
DRAWN KG.	ISSUE No. 1
CHECKED	AR No. 1588
APPROVED	DATE 26-8-66
DATE	INITIALS KG

ELLIOTT BROTHERS (LONDON) LTD.

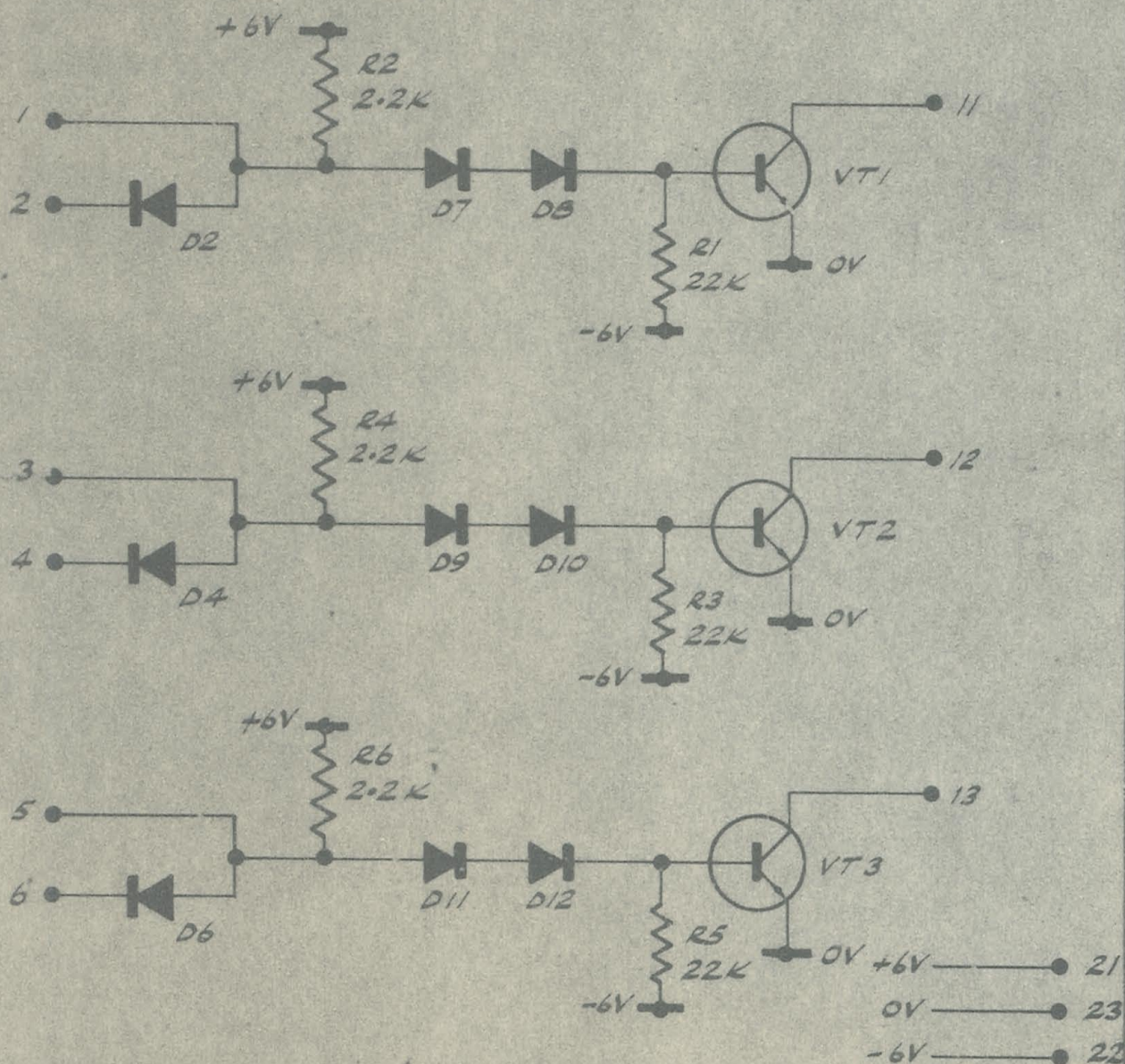
LSA 43
VOLTAGE RAIL SENSING

INSTRUCTION SHEET
322 A 7191

SHEET No 28
OF



DIODES ARE PURCH-101
TRANSISTORS ARE PURCH-100



AVR N.G.R.H. ISSUE No. 1
POWER CS P.H.S. PAR. No.
892 P.H.S. DATE 26.11.66
INITIAL J.H.

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LSA 44
2-INPUT NANDGATE 920B
(USED IN CONJUNCTION WITH LSA23)

INSTRUCTION SHEET

322A7191

SHEET No 29
OF